Rev A, January 2026

1. 特性

- 输出配置
  - 立体声 2.0: 2 × 32W (8Ω, 24V, THD+N = 1%)
  - 立体声 2.0: 2 × 23W (6Ω, 18V, THD+N = 1%)
- 供电电压范围
  - PVDD: 4.5V 至 26.4V
  - DVDD: 1.8V 或者 3.3V
- 静态功耗
  - 29mA at PVDD = 12V, BD
  - 18mA at PVDD = 12V, 1SPW
- 音频性能指标
  - Noise: ≤ 38μV_{RMS}
  - THD+N ≤ 0.03% at 1W, 1kHz
  - SNR ≥ 108dB (A-weighted)
  - DC offset ≤ ±5mV
- 音频输入信号格式
  - 3-wire I^2S, LJ, RJ, TDM (无需 MCLK)
  - Fs 支持 32/44.1/48/88.2/96/176.4/192kHz 采样率
  - 支持独立回声消除通道 Sdout
- 音频 DSP 算法
  - 2 × 15 EQs + 3-band DRC + AGL + 3 × post EQs
  - 支持动态低音增强算法
  - 配合外部 boost 电路支持 Class H 算法
- 控制模式
  - 支持 I^2C 软件配置模式
  - 支持硬件 IO 控制模式，无需 I^2C 寄存器控制
- 保护功能
  - 过流/过压(28V)/过温/欠压/直流保护
  - 过流保护门限 8A
  - 实时供电电压/芯片温度监测可读出
  - 支持系统级热管理保护
- 调音及系统集成
  - 一站式 GUI 调音软件 ASATP，驱动级整体解决方案
  - 支持上位机一键生成配置文件

2. 应用

- 专业音响设备
- 智能音箱
- 条形音响
- 电视
- 笔记本电脑
- 会议系统

3. 描述

AU6815E 是一款数字输入型、双通道立体声、高效的音频 Class-D 功率放大器，其最大输出功率可达 2 × 32W 或 1 × 64W。

AU6815E 采用创新的调制模式，可以有效降低静态功耗，提升续航时间。AU6815E 内部集成有 32 位的高精度音频 DSP，可提供包括 2 × 15 个均衡器，3 段 DRC 以及 AGL 等调音算法。此外，为了进一步增强小音量下的低音表现，AU6815E 还支持动态低音增强算法 DPEQ。AU6815E 内部 DSP 处理带宽最大支持 48kHz (96kHz 采样率)。

在音质表现方面，AU6815E 的 THD+N 指标可以达到 0.03% 以下的水平，此外极低的直流偏置电压使得 AU6815E 在开机关机 pop 音方面具备极其出色的性能。

作为一款中大功率音频功率放大器，AU6815E 在热管理方面支持四档过温报警和过温度关断保护。此外，该芯片温度可以通过寄存器连续输出，方便系统做整体热管理。在喇叭保护方面，AU6815E 还支持过流/过压/欠压/直流保护等。

AU6815E 支持 TSSOP28PP 封装，无需散热片，其额定温度范围为–25°C 至+85°C。有关订购信息，参见 Table 1。

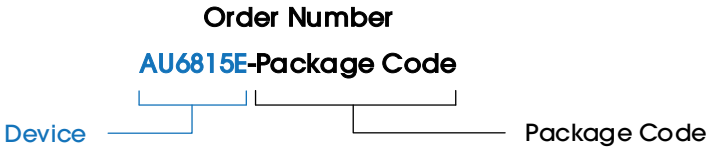
Table 1 lists the order information.

Table 1. Order Information

ORDER NUMBER(1)	PART NUMBER	CH (#)	PACKAGE	MARK(2)	OUTPUT POWER (W)	DIGITAL INPUT	PVDD (TYP) (V)	OPERATING TEMP (°C)	MSL	PACKAGE OPTION
AU6815EATSSOP28P	AU6815E	2	TSSOP28PP	AU6815E XXXXXX	2 × 32	Yes	26.4	–25-85	2	3000

Devices can be ordered via the following two ways:
1. Place orders directly on our website (www.analogysemi.com), or;
2. Contact our sales team by mailing to sales@analogysemi.com.

Note 1:



Note 2: "XXXXXX": For internal use.

4. PIN CONFIGURATION AND FUNCTIONS

Figure 1 illustrates the pin configuration.

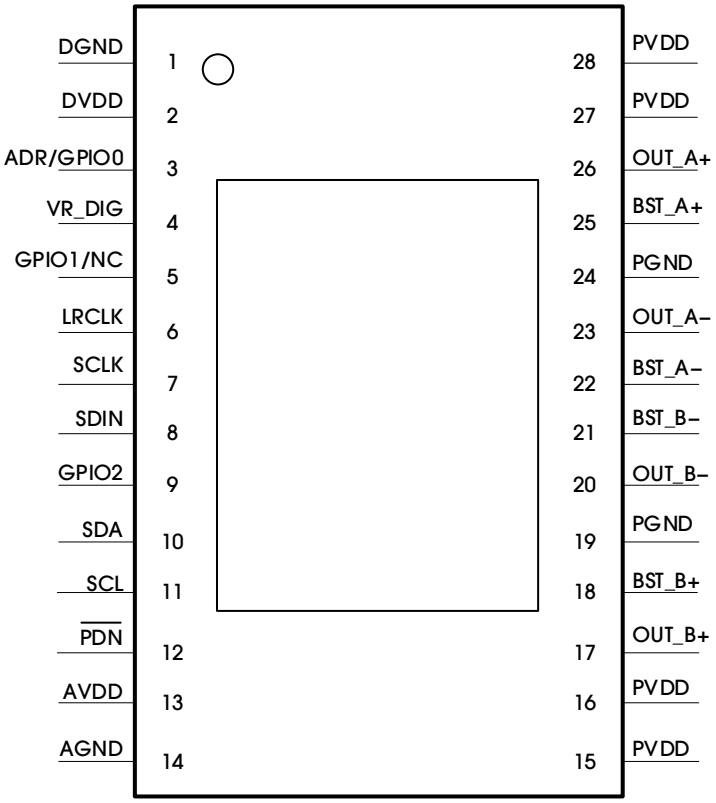


Figure 1. Pin Configuration

Table 2 lists the pin functions.

Table 2. Pin Functions

POSITION	NAME	TYPE(1)	DESCRIPTION
1	DGND	P	Digital ground
2	DVDD	P	3.3V or 1.8V digital power supply
3	ADR/GPIO0	DI/O	Different I²C device address can be set by selecting different pull-up resistor to DVDD. Alternatively, it can be used as GPIO0 and can be configured as FAULT.
4	VR_DIG	P	Internally regulated 1.8V digital supply voltage. This pin must NOT be used to drive external devices.
5	GPIO1/NC	DI/O	Optional for GPIO1 or NC or DGND
6	LRCLK	DI	Word select clock for the digital signal that is active on the serial port's input data line. In I²S, LJ, and RJ, this corresponds to the left channel and right channel boundary. In the TDM mode, this corresponds to the frame sync boundary.
7	SCLK	DI	Bit clock for the digital signal that is active on the input data line of the serial data port.
8	SDIN	DI	Data line to the serial data port
9	GPIO2	DO	Default as serial audio data output Sdout or used as a common GPIO with multiple functions
10	SDA	DI/O	I²C serial control data interface input/output
11	SCL	DI	I²C serial control clock input
12	$\overline{\text{PDN}}$	DI	Power-down, active-low. $\overline{\text{PDN}}$ places the amplifier in Shutdown, and turns off all internal regulators. Low—Power down device; High—Enable device.
13	AVDD	P	Internally regulated 5V analog supply voltage. This pin must NOT be used to drive the external devices.
14	AGND	P	Analog ground
15, 16, 27, 28	PVDD	P	PVDD voltage input

POSITION	NAME	TYPE(1)	DESCRIPTION
17	OUT_B+	O	Positive pin for differential speaker amplifier output B+
18	BST_B+	P	Connection point for the OUT_B+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B+
19, 24	PGND	P	Ground reference for power device circuitry. Connect this pin to system ground.
20	OUT_B–	O	Negative pin for differential speaker amplifier output B
21	BST_B–	P	Connection point for the OUT_B– bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B–
22	BST_A–	P	Connection point for the OUT_A– bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A–
23	OUT_A–	O	Negative pin for differential speaker amplifier output A–
25	BST_A+	P	Connection point for the OUT_A+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A+
26	OUT_A+	O	Positive pin for differential speaker amplifier output A+
—	PowerPAD	P	Connect to the system ground

Note: AI = analog input, AO = analog output, DI = digital input, DO = digital output, DI/O = digital bi-directional (input and output), P = power, G = ground (0V).

5. SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Table 3 lists the absolute maximum ratings of the AU6815E.

Table 3. Absolute Maximum Ratings

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
Voltage	Low-voltage digital supply, DVDD	–0.3	3.9	V
	PVDD supply, PVDD	–0.3	32	
	DVDD referenced digital inputs(2), $V_{I(DigIn)}$	–0.3	V_{DVDD} + 0.5	
	Voltage at speaker output pins, $V_{I(SPK\_OUTxx)}$	–0.3	32	
Resistance	Load resistance, R_L	2.4		Ω
Temperature	Ambient operating, T_A	–25	85	°C
	Junction, T_j	–40	180	
	Storage, T_{stg}	–40	125	

Note 1: Stresses beyond those listed under Table 3 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 5. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 2: DVDD referenced digital pins include: ADR/$\overline{\text{FAULT}}$, LRCLK, SCLK, SCL, SDA, SDIN, and $\overline{\text{PDN}}$.

5.2 ESD RATINGS

Table 4 lists the ESD ratings of the AU6815E.

Table 4. ESD Ratings

PARAMETER	SYMBOL	DESCRIPTION	VALUE	UNITS
Electrostatic Discharge	$V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

Note 1: The JEDEC document JEP155 indicates that 500V HBM allows safe manufacturing with a standard ESD control process.

Note 2: The JEDEC document JEP157 indicates that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 RECOMMENDED OPERATING CONDITIONS

Table 5 lists the recommended operating conditions for the AU6815E.

Table 5. Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNITS
Power Supply Inputs	$V_{(POWER)}$	DVDD	1.65		3.63	V
		PVDD	4.5		26.4	V
Minimum Speaker Load	R_{SPK}	BTL mode (4.5V ≤ PVDD ≤ 16V)	3			Ω
		BTL mode (16V ≤ PVDD ≤ 24V)	4			Ω
		PBTL mode (4.5V ≤ PVDD ≤ 16V)	1.5			Ω
		PBTL mode (16V ≤ PVDD ≤ 24V)	2			Ω
Minimum Inductor Value in LC Filter under Short-Circuit Condition	L_{OUT}		1	4.7		μH
Junction Temperature	T_J		–40		150	°C

Note: The minimal speaker load is limited by the OCE threshold. If output peak current < 8A, the AU6815E also supports lower speaker load with high PVDD. For BTL, the OCE threshold is 8A (typical); For PBTL, the OCE threshold is 16A (typical). The minimal speaker load depends on the output peak voltage.

5.4 THERMAL INFORMATION

Table 6 lists the thermal information for the AU6815E.

Table 6. Thermal Information

PARAMETER	SYMBOL	TSSOP28PP	UNITS
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	30	°C/W
Junction-to-Board Thermal Resistance	$R_{\theta JB}$	11	°C/W
Junction-to-Top Characterization Parameter	Ψ_{JT}	0.3	°C/W
Junction-to-Board Characterization Parameter	Ψ_{JB}	11	°C/W
Junction-to-Case (Top) Thermal Resistance	$R_{\theta JC\ (top)}$	13	°C/W
Junction-to-Case (Bottom) Thermal Resistance	$R_{\theta JC\ (bot)}$	2	°C/W

5.5 ELECTRICAL CHARACTERISTICS

Table 7 lists the electrical characteristics of the AU6815E. Free-air room temperature 25°C, unless otherwise noted.

Table 7. Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL I/O						
Input Logic High Current Level for DVDD Referenced Digital Input Pins	$\|I_{IH}\|$	$V_{IL(Digin)} = V_{DVDD}$			5	μA
Input Logic Low Current Level for DVDD Referenced Digital Input Pins	$\|I_{IL}\|$	$V_{IL(Digin)} = 0V$			–5	μA
Input Logic High Threshold for DVDD Referenced Digital Inputs	$V_{IH(Digin)}$		70%			V_{DVDD}
Input Logic Low Threshold for DVDD Referenced Digital Inputs	$V_{IL(Digin)}$				30%	V_{DVDD}
Output Logic High Voltage Level	$V_{OH(Digin)}$	I_{OH} = 2mA	80%			V_{DVDD}
Output Logic Low Voltage Level	$V_{OL(Digin)}$	I_{OH} = –2mA			20%	V_{DVDD}
I²C CONTROL PORT						
Allowable Load Capacitance for Each I²C Line	$C_{L(I2C)}$				400	pF
Support SCL Frequency	$f_{SCL(fast)}$	No wait states, fast mode			400	kHz
Support SCL Frequency	$f_{SCL(slow)}$	No wait states, slow mode			100	kHz
SERIAL AUDIO PORT						
Required LRCLK/FS to SCLK Rising Edge Delay	t_{DLY}		5			ns
Allowable SCLK Duty Cycle	D_{SCLK}		40%		60%	
Supported Input Sample Rates	f_S		32		192	kHz
Supported SCLK Frequencies	f_{SCLK}		32		64	f_S
SCLK Frequency	f_{SCLK}				24.576	MHz
SPEAKER AMPLIFIER (ALL OUTPUT CONFIGURATIONS)						
Quiescent Supply Current on PVDD	I_{cc}	$\overline{PDN}$ = 2V, PVDD = 12V, LC filter = 10μH + 0.68μF, F_{SW} = 768kHz, BD modulation, Play mode		29		mA
Quiescent Supply Current on PVDD	I_{cc}	$\overline{PDN}$ = 2V, PVDD = 12V, LC filter = 10μH + 0.68μF, F_{SW} = 768kHz, 1SPW, Play mode		18		mA
Quiescent Supply Current on PVDD	I_{cc}	$\overline{PDN}$ = 2V, PVDD = 12V, Output Hi-Z mode		7		mA
Quiescent Supply Current on PVDD	I_{cc}	$\overline{PDN}$ = 2V, PVDD = 12V, Sleep mode		2		mA
Quiescent Supply Current on PVDD	I_{cc}	$\overline{PDN}$ = 2V, PVDD = 12V, Deep Sleep mode		4		μA
Quiescent Supply Current on PVDD	I_{cc}	$\overline{PDN}$ = 0V, PVDD = 12V, Shutdown		3.8		μA
Quiescent Supply Current on DVDD	I_{cc}	PDN = 2V, DVDD = 3.3V, Play mode and Hi-Z mode		16.5		mA
Quiescent Supply Current on DVDD	I_{cc}	PDN = 2V, DVDD = 3.3V, Sleep mode and Deep Sleep mode		0.8		mA
Quiescent Supply Current on DVDD	I_{cc}	PDN = 0V, DVDD = 3.3V, Shutdown mode		1.4		μA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Turn-Off Time	t_{off}	Excluding volume ramp			10	ms
Programmable Gain	$A_{V(SPK\_AMP)}$	Value represents the "peak voltage" disregarding clipping due to lower PVDD. Measured at 0dB input (1FS).	4.87		29.5	V
Amplifier Gain Error	$\Delta A_{V(SPK\_AMP)}$	Gain = 26Vp/FS		0.1		dB
Switching Frequency of the Speaker Amplifier	f_{SPK_AMP}			260		kHz
				768		kHz
Drain-to-Source on Resistance of the Individual Output MOSFETs	$R_{DS(on)}$	FET + Metallization		110		mΩ
Overcurrent Error Threshold	OCE_{THRES}	OUTxx overcurrent error threshold	6.8	8		A
PVDD Overvoltage Error Threshold	$OVE_{THRES(PVDD)}$			28		V
PVDD Undervoltage Error Threshold	$UVE_{THRES(PVDD)}$			4.2		V
Overtemperature Error Threshold	OTE_{THRES}			160		°C
Overtemperature Error Hysteresis	$OTE_{Hystersis}$			15		°C
Overtemperature Warning Level 1	OTW_{THRES1}	Read by register 0x73 bit 3		146		°C
Overtemperature Warning Level 2	OTW_{THRES2}	Read by register 0x73 bit 2		135		°C
Overtemperature Warning Level 3	OTW_{THRES3}	Read by register 0x73 bit 1		125		°C
Overtemperature Warning Level 4	OTW_{THRES4}	Read by register 0x73 bit 0		113		°C
SPEAKER AMPLIFIER (STEREO BTL)						
Amplifier Offset Voltage	$\lvert V_{OS} \rvert$	Measured differentially with zero input data, programmable gain configured with 29.5Vp gain, V_{PVDD} = 12V, BD mode	–5		5	mV
Continuous Output Power (per Channel)	$P_{O(SPK)}$	V_{PVDD} = 12V, RSPK = 4Ω, f = 1kHz, THD+N = 1%		13.8		W
		V_{PVDD} = 12V, RSPK = 4Ω, f = 1kHz, THD+N = 10%		17		W
		V_{PVDD} = 18V, RSPK = 6Ω, f = 1kHz, THD+N = 1%		23.4		W
		V_{PVDD} = 18V, RSPK = 6Ω, f = 1kHz, THD+N = 10%		28		W
		V_{PVDD} = 24V, RSPK = 8Ω, f = 1kHz, THD+N = 1%		32		W
		V_{PVDD} = 24V, RSPK = 8Ω, f = 1kHz, THD+N = 10%		40		W
Total Harmonic Distortion and Noise (P_O = 1W, f = 1kHz, R_{SPK} = 6Ω)	$THD+N_{SPK}$	V_{PVDD} = 12V, F_{SW} = 768kHz, SPK_GAIN = 13.9Vp/FS, LC-filter, BD mode		0.02		%
		V_{PVDD} = 18V, F_{SW} = 768kHz, SPK_GAIN = 20.8Vp/FS, LC-filter, BD mode		0.02		%
Idle Channel Noise (A-Weighted)	$I_{CN(SPK)}$	V_{PVDD} = 12V, F_{SW} = 768kHz, LC-filter, load = 6Ω		34		μV_{RMS}
		V_{PVDD} = 18V, F_{SW} = 768kHz, LC-filter, load = 6Ω		38		
Dynamic Range	DR	A-Weighted, –60dBFS method. PVDD = 24V, SPK_GAIN = 29.5Vp/FS		114		dB

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Signal-to-Noise Ratio	SNR	A-Weighted, referenced to 1% THD+N output level, PVDD = 12V		110		dB
Power Supply Rejection Ratio	K_{SVR}	Injected noise = 1kHz, $1V_{RMS}$, PVDD = 12V, input audio signal = digital zero		72		dB
Crosstalk (Worst Case between Left-to-Right and Right-to-Left Coupling)	$X\text{-}talk_{SPK}$	f = 1kHz		92		dB
SPEAKER AMPLIFIER (MONO PBTL)						
Total Harmonic Distortion and Noise (P_O = 1W, f = 1kHz)	$THD+N_{SPK}$	V_{PVDD} = 12V, SPK_GAIN = 16.5Vp/FS, 10μH + 0.68μF filter, R_{SPK} = 4Ω, BD mode		0.03%		
		V_{PVDD} = 24V, SPK_GAIN = 29.5Vp/FS, 10μH + 0.68μF filter, R_{SPK} = 4Ω, 1SPW mode		0.04%		
Signal-to-Noise Ratio	SNR	A-weighted, referenced to 1% THD+N output level, PVDD = 12V		109		dB
Power Supply Rejection Ratio	K_{SVR}	Injected noise = 1kHz, $1V_{RMS}$, PVDD = 12V, input audio signal = digital zero		72		dB

5.6 TIMING REQUIREMENTS

Table 8 lists the timing requirements.

Table 8. Timing Requirements

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS
SERIAL AUDIO PORT TIMING					
SCLK Frequency	f_{SCLK}	1.024			MHz
SCLK Period	t_{SCLK}	40			ns
SCLK Pulse Width, Low	t_{SCLKL}	16			ns
SCLK Pulse Width, High	t_{SCLKH}	16			ns
SCLK Rising to LRCK/FS Edge	t_{SL}	8			ns
LRCK/FS Edge to SCLK Rising Edge	t_{LS}	8			ns
Data Setup Time, Before SCLK Rising Edge	t_{SU}	8			ns
Data Hold Time, After SCLK Rising Edge	t_{DH}	8			ns
Data Delay Time from SCLK Falling Edge	t_{DFS}			18	ns
I^2C BUS TIMING – STANDARD					
SCL Clock Frequency	f_{SCL}			100	kHz
Bus Free Time Between A STOP and START Condition	t_{BUF}	4.7			μs
Low Period of the SCL Clock	t_{LOW}	4.7			μs
High Period of the SCL Clock	t_{HI}	4			μs
Setup Time for (Repeated) START Condition	t_{RS-SU}	4.7			μs
Hold Time for (Repeated) START Condition	t_{S-HD}	4			μs
Data Setup Time	t_{D-SU}	250			ns
Data Hold Time	t_{D-HD}	0		3450	ns
Rise Time of SCL Signal	t_{SCL-R}	$20 + 0.1C_B$		1000	ns
Rise Time of SCL Signal After A Repeated START Condition and After An Acknowledge Bit	t_{SCL-R1}	$20 + 0.1C_B$		1000	ns
Fall Time of SCL Signal	t_{SCL-F}	$20 + 0.1C_B$		1000	ns
Rise Time of SDA Signal	t_{SDA-R}	$20 + 0.1C_B$		1000	ns
Fall Time of SDA Signal	t_{SDA-F}	$20 + 0.1C_B$		1000	ns
Setup Time for STOP Condition	t_{P-SU}	4			μs
Capacitive Load for Each Bus Line	C_B			400	pF
I^2C BUS TIMING – FAST					
SCL Clock Frequency	f_{SCL}			400	kHz
Bus Free Time Between A STOP and START Condition	t_{BUF}	1.3			μs
Low Period of the SCL Clock	t_{LOW}	1.3			μs
High Period of the SCL Clock	t_{HI}	600			ns
Setup Time for (Repeated) START Condition	t_{RS-SU}	600			ns
Hold Time for (Repeated) START Condition	t_{RS-HD}	600			ns
Data Setup Time	t_{D-SU}	100			ns
Data Hold Time	t_{D-HD}	0		900	ns
Rise Time of SCL Signal	t_{SCL-R}	$20 + 0.1C_B$		300	ns
Rise Time of SCL Signal After A Repeated START Condition and After An Acknowledge Bit	t_{SCL-R1}	$20 + 0.1C_B$		300	ns
Fall Time of SCL Signal	t_{SCL-F}	$20 + 0.1C_B$		300	ns
Rise Time of SDA Signal	t_{SDA-R}	$20 + 0.1C_B$		300	ns
Fall Time of SDA Signal	t_{SDA-F}	$20 + 0.1C_B$		300	ns
Setup Time for STOP Condition	t_{P-SU}	600			ns
Pulse Width of Spike Suppressed	t_{SP}			50	ns
Capacitive Load for Each Bus Line	C_B			400	pF

6. TYPICAL CHARACTERISTICS

Free-air room temperature 25°C (unless otherwise noted). Measurements were made using the AU6815E EVM board and Audio Precision System 555 with Analog Analyzer filter set to 20kHz brickwall filter. All measurements were taken with audio frequency set to 1kHz unless otherwise noted.

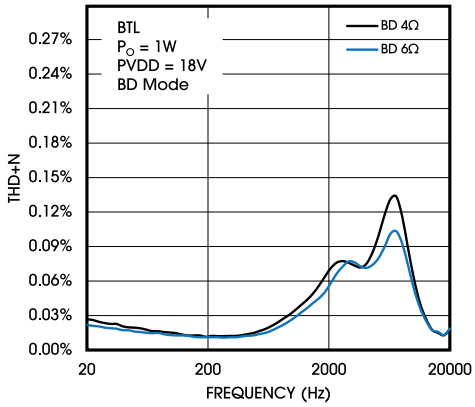


Figure 2. THD+N vs. Frequency (BTL)

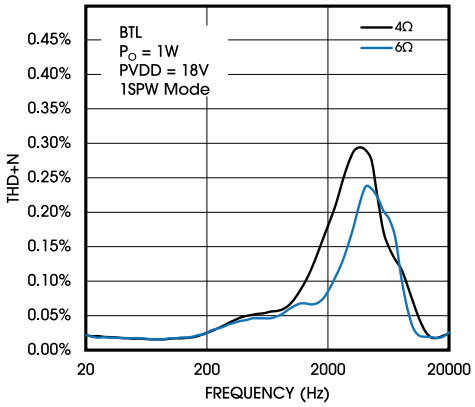


Figure 3. THD+N vs. Frequency (BTL)

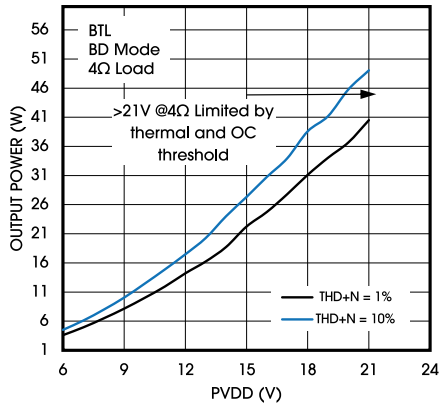


Figure 4. Output Power vs. Supply Voltage (BTL)

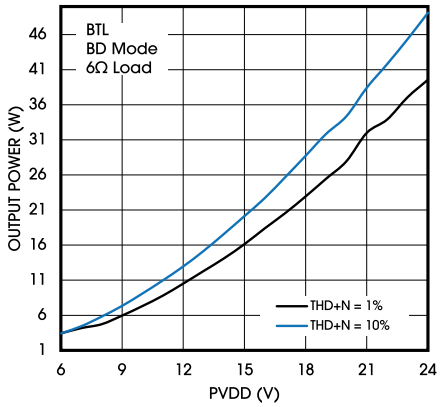


Figure 5. Output Power vs. Supply Voltage (BTL)

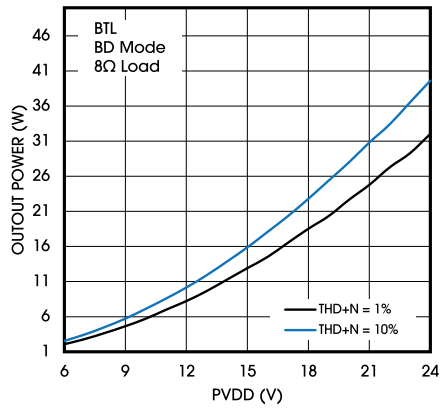


Figure 6. Output Power vs. Supply Voltage (BTL)

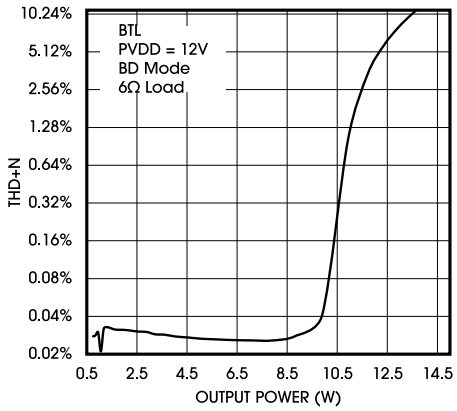


Figure 7. THD+N vs. Output Power (BTL)

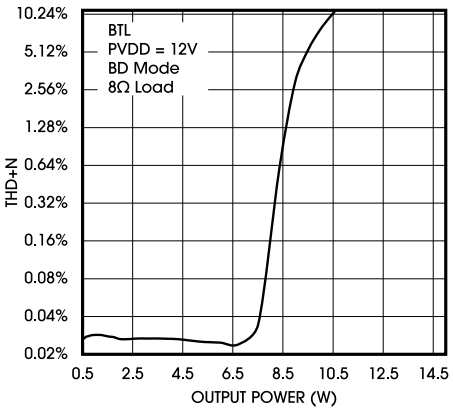


Figure 8. THD+N vs. Output Power (BTL)

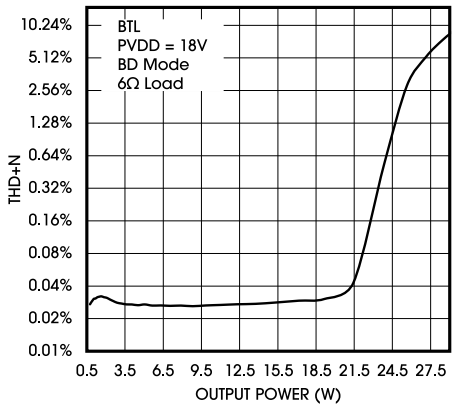


Figure 9. THD+N vs. Output Power (BTL)

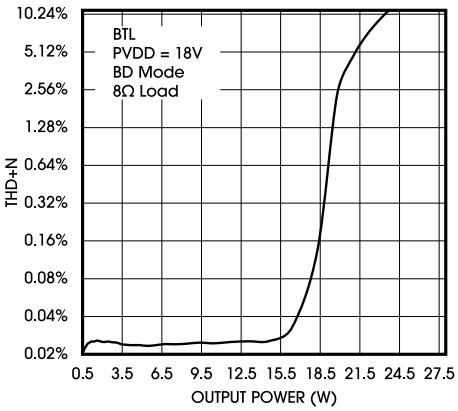


Figure 10. THD+N vs. Output Power (BTL)

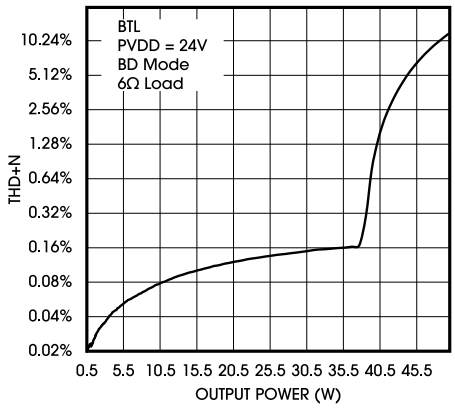


Figure 11. THD+N vs. Output Power (BTL)

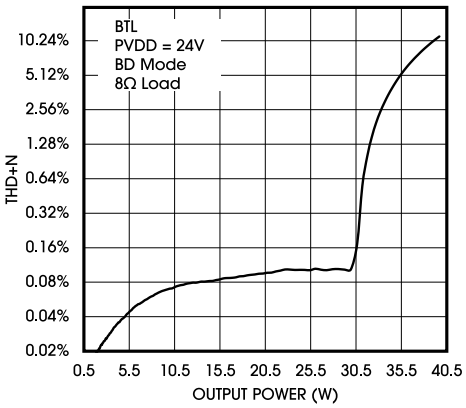


Figure 12. THD+N vs. Output Power (BTL)

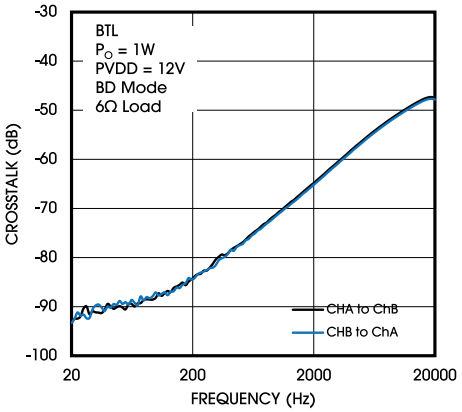


Figure 13. Crosstalk (BTL)

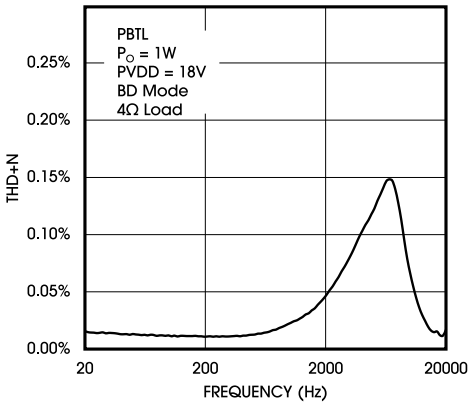


Figure 14. THD+N vs. Frequency (PBTL)

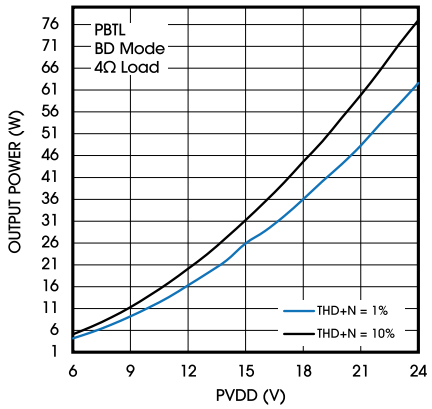


Figure 15. Output Power vs. Supply Voltage (PBTL)

7. 参数测量信息

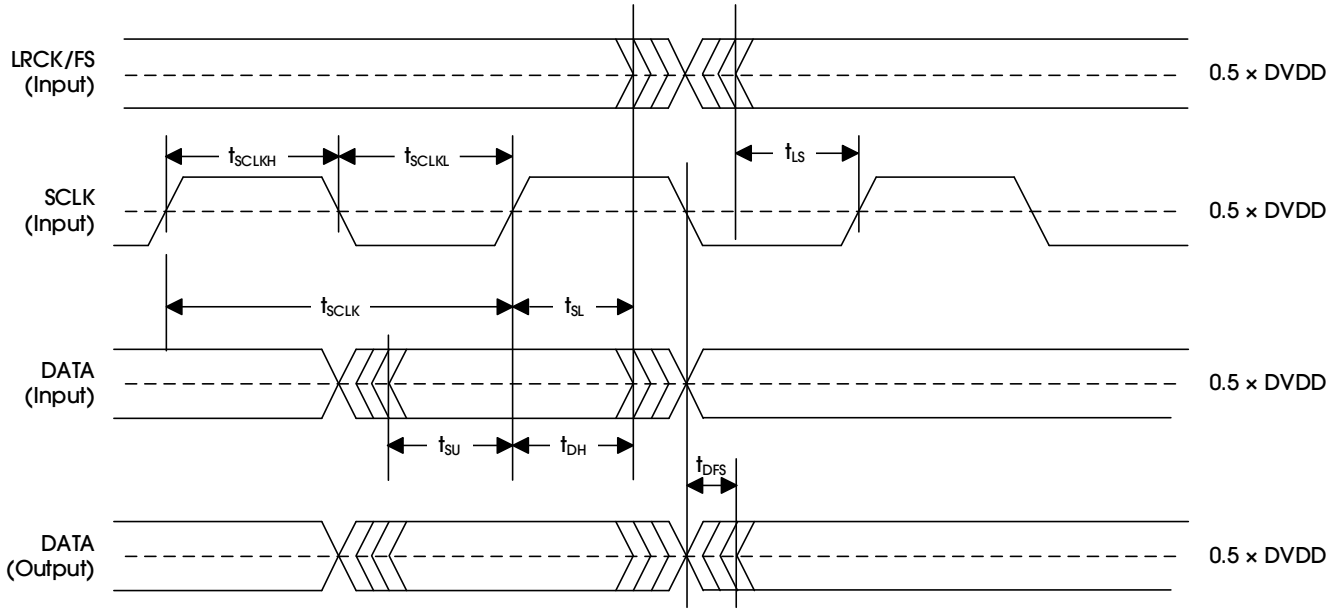


Figure 16. Serial Audio Port Timing in Slave Mode

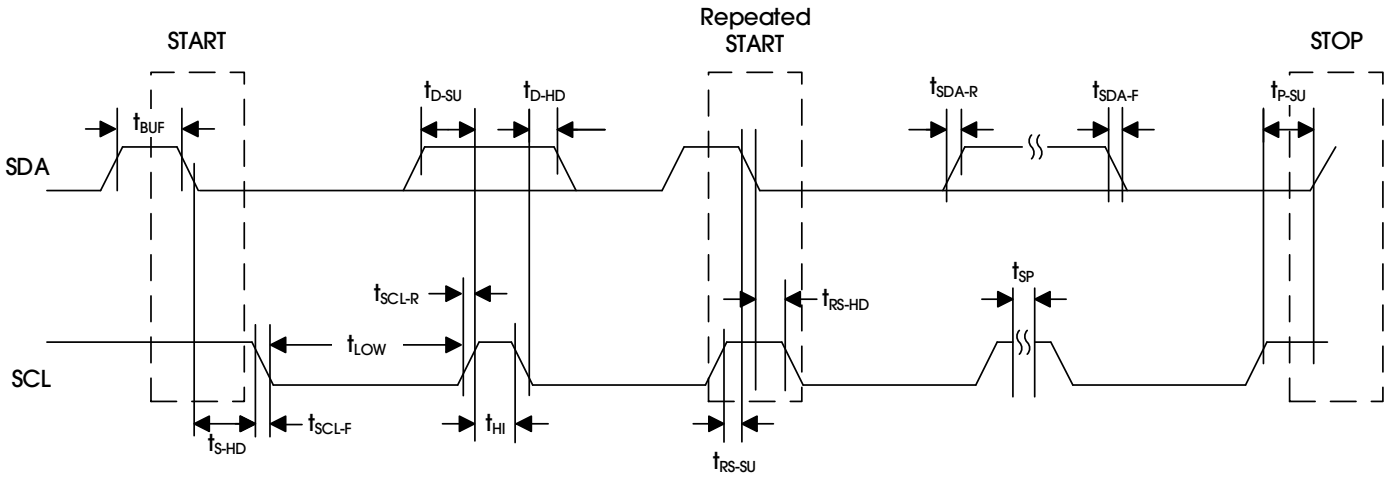


Figure 17. I²C Communication Port Timing Diagram

8. 详细说明

8.1 概述

AU6815E 主要由 5 个部分组成，包括：

- 一个立体声 DAC
- 32-bit 高精度音频 DSP
- 闭环架构的 Class-D
- I^2C 控制接口
- 保护逻辑和内部 ADC 电压温度采样模块

PVDD 供电电压范围为 4.5V 到 26.4V，DVDD 支持 3.3V 或者 1.8V 逻辑。AU6815E 提供两个 GPIO，可以配置成回声消除或者其他 GPIO 功能，例如 fault。此外，AU6815E 还支持 32k-192k 输入采样率。

8.2 功能模块框图

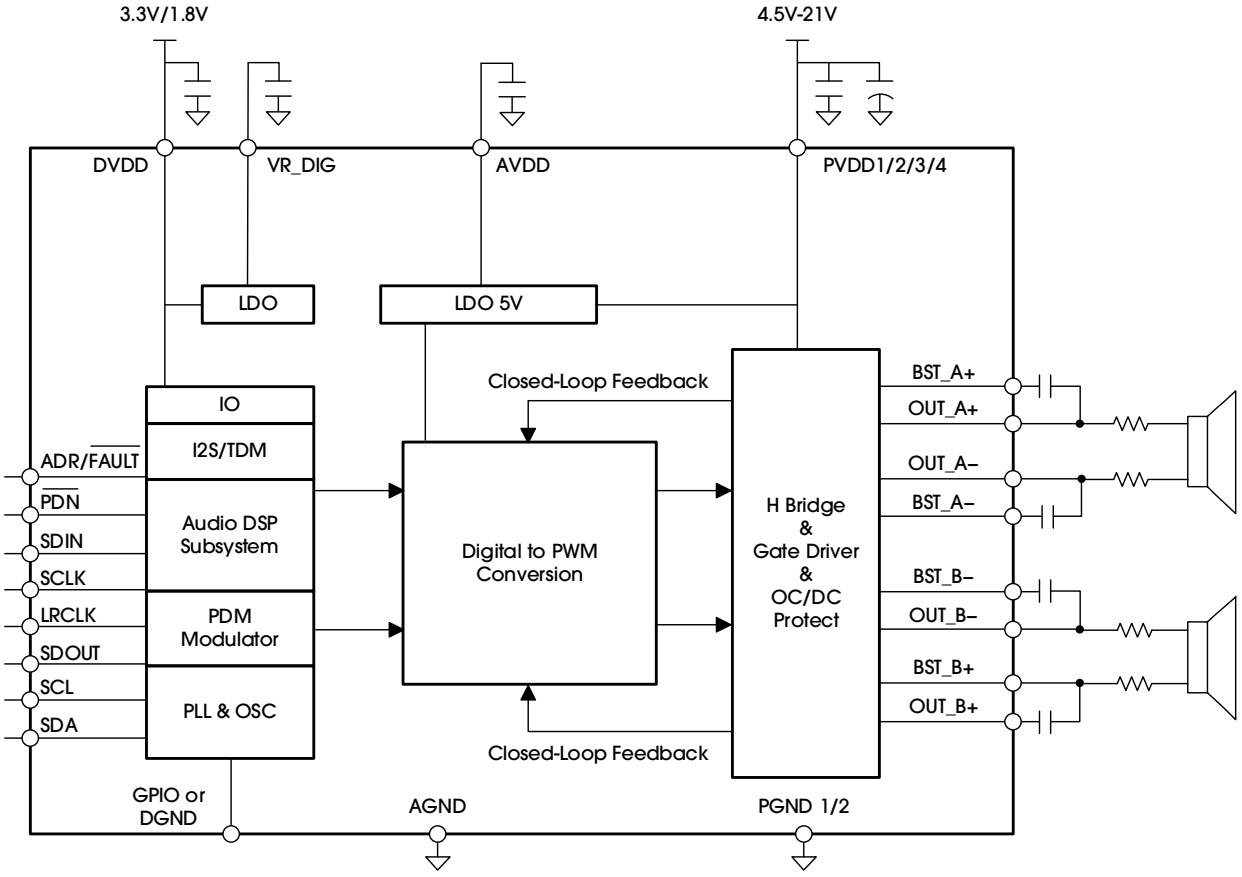


Figure 18. Functional Block Diagram

8.3 特性描述

8.3.1 串行音频接口及频率

AU6815E 支持的音频输入数据格式和频率配置如 Table 9 所示。

Table 9. Audio Data Formats, Bit Depths, and Clock Rates

FORMAT	DATA BITS	MAXIMUM LRCLK/FS FREQUENCY (kHz)	SCLK RATE (F_S)
I^2S/LJ/RJ	32, 24, 20, 16	32 to 96	64, 32
TDM	32, 24, 20, 16	32	128
		44.1, 48	128, 256, 512
		96	128, 256

8.3.2 时钟停止及恢复

AU6815E 支持时钟频率停止后自动进入 Hi-Z 或者其他低功耗模式，时钟恢复后可以自动恢复。

8.3.3 在线改变采样率

AU6815E 支持在线编辑 EQ 等参数，此外还支持自动切换采样率功能。通常情况为了避免 pop 音，建议进入 Hi-Z 或者 sleep 等状态后再进行采样率切换。

8.3.4 串行音频接口-数据格式和有效位

AU6815E 支持如下 I^2S 格式：

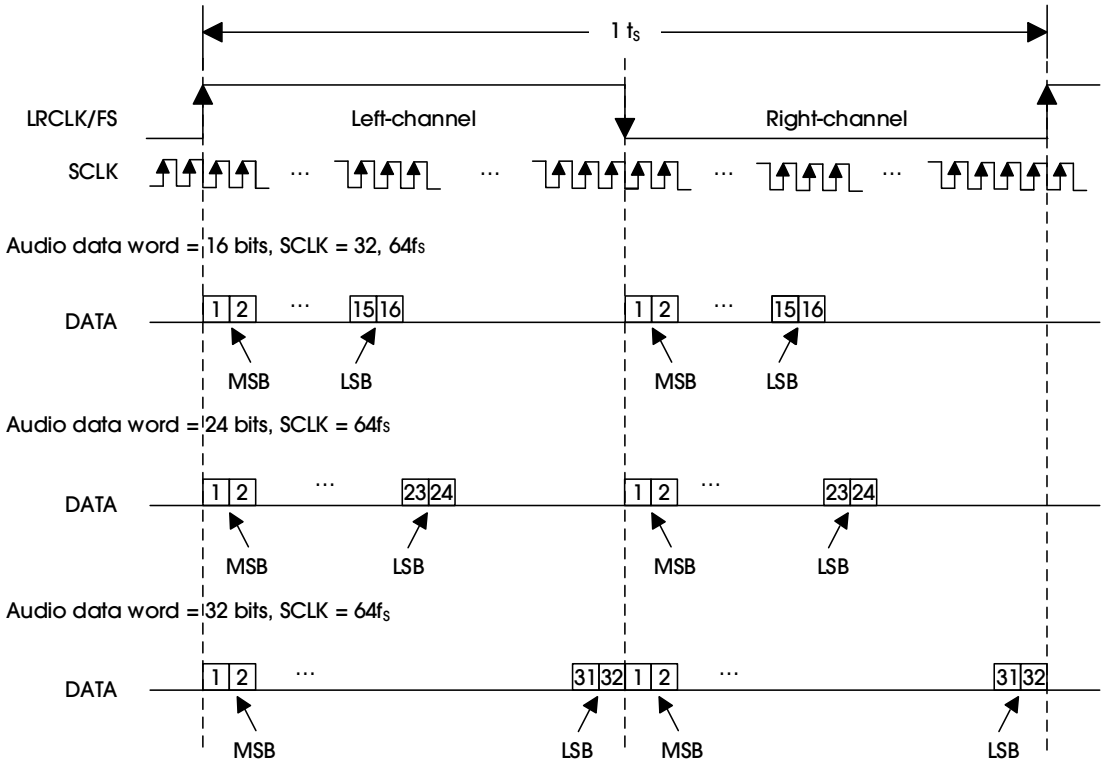
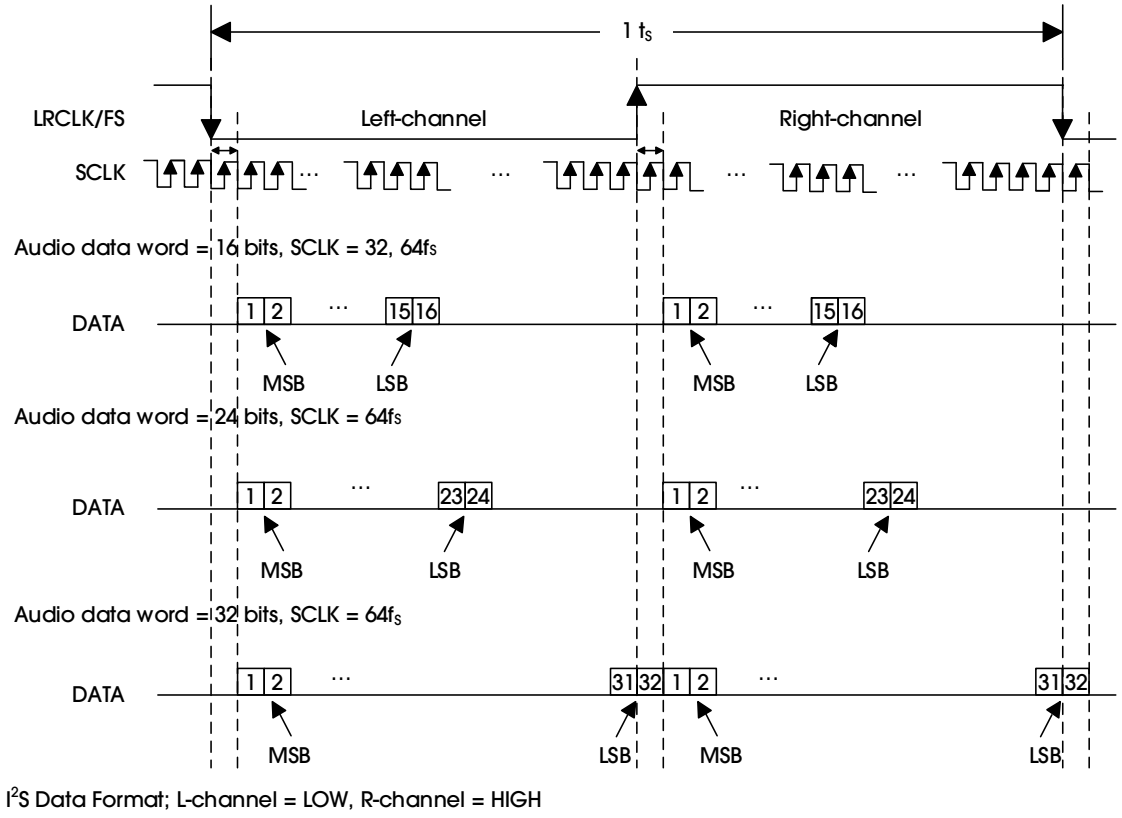
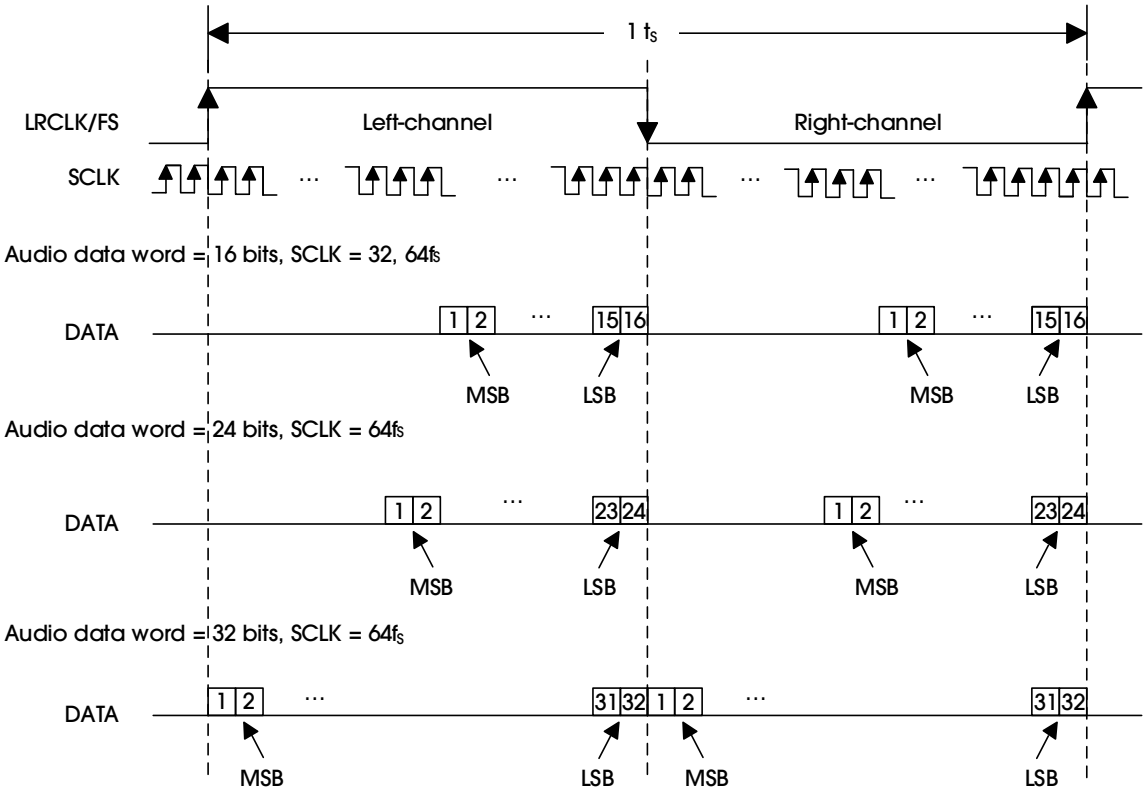


Figure 19. Left-Justified Audio Data Format



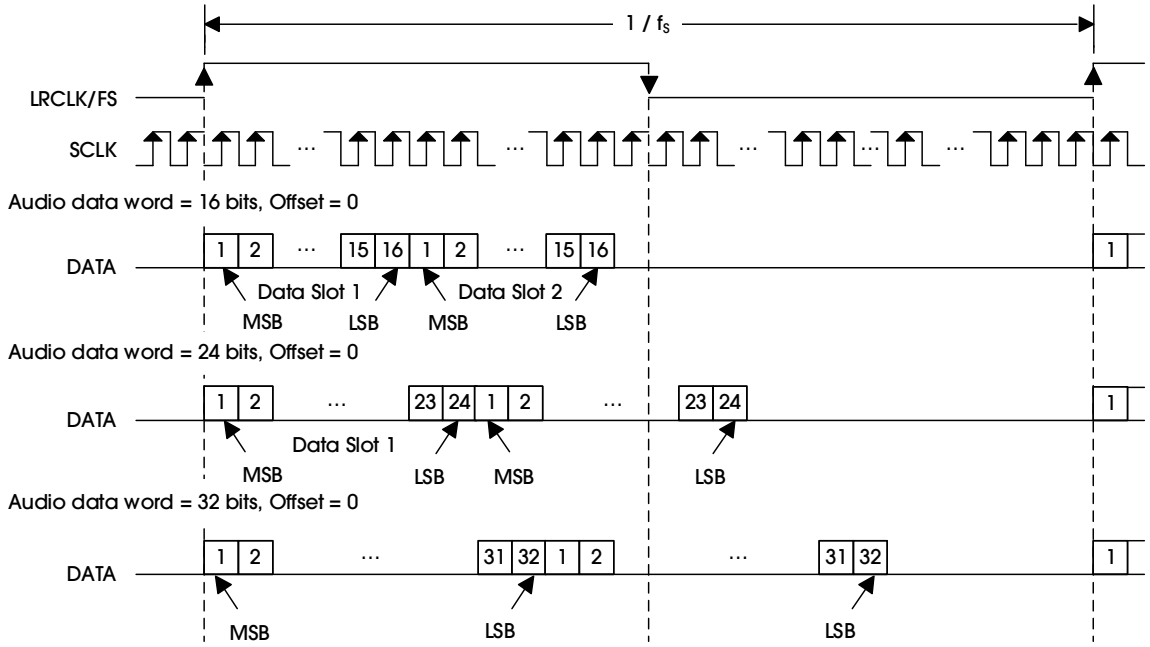
I²S Data Format; L-channel = LOW, R-channel = HIGH

Figure 20. I²S Audio Data Format



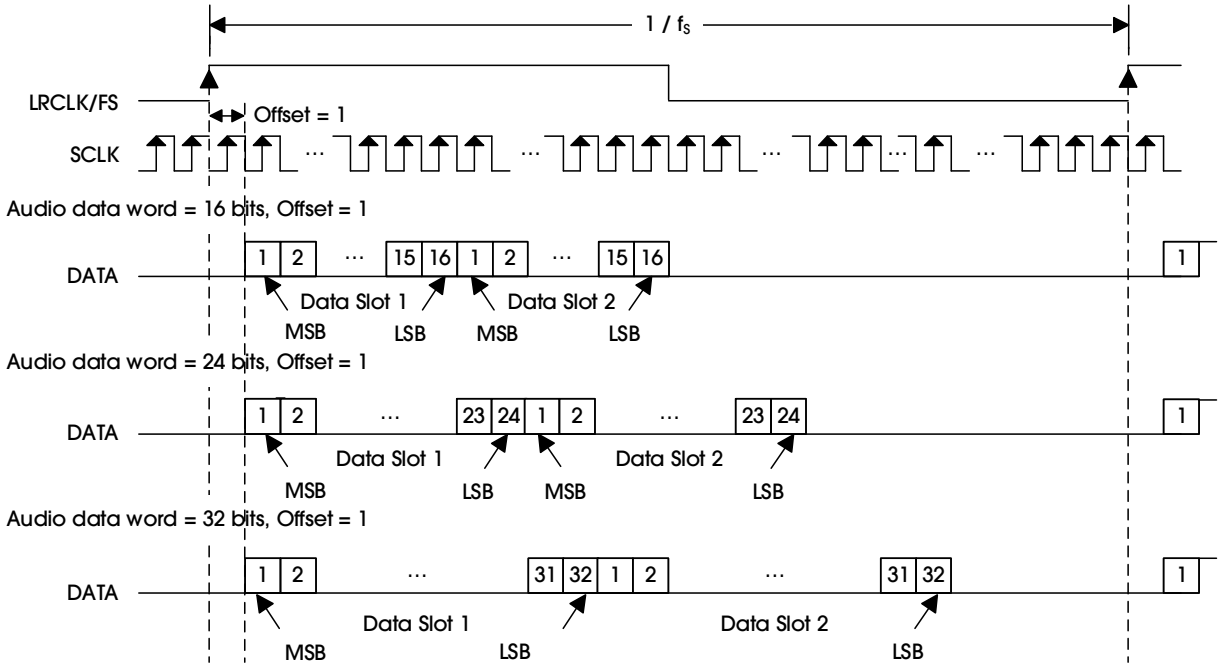
Right-Justified Data Format; L-channel = HIGH, R-channel = LOW

Figure 21. Right-Justified Audio Data Format



TDM data format with OFFSET = 0
In TDM modes, duty cycle of LRCLK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

Figure 22. TDM 1 Audio Data Format



TDM data format with OFFSET = 1
In TDM modes, duty cycle of LRCLK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

Figure 23. TDM 2 Audio Data Format

8.3.5 数字音频处理

AU6815E DSP 支持多种音频处理的算法结构，配置上包括立体声 2.0、高低音 1.1、2.1 或者 2.2 模式。

1. 简单模式：SRC + 2 × 15 × EQ + 1-band DRC + AGL
2. 标准模式：SRC + 2 × 15 EQs + 3-band DRC + AGL + 3 post-EQ
3. 高阶模式：SRC + 2 × 15 EQs + DPEQ + 3-band DRC + AGL + 3 post-EQ

类比半导体提供一站式调音平台，该平台可以直接产生配置脚本。

8.3.6 功放增益选择

功放基本框图如 Figure 24 所示：

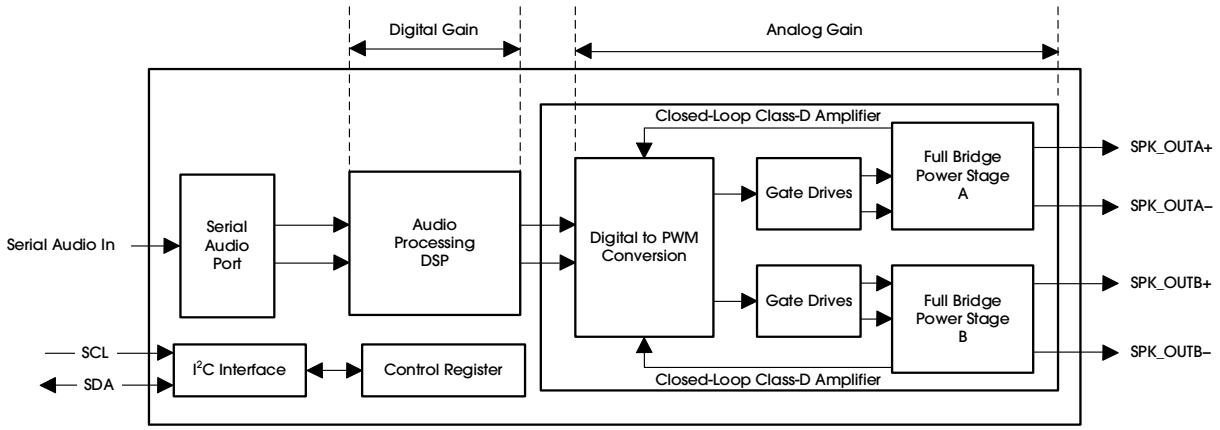


Figure 24. Speaker Amplifier Gain

配置增益主要通过模拟的增益，即寄存器 0x54, Book 0, Page 0。其对应的输出 peak 值如 Table 10 所示。此外，DSP 部分也可以配置增益，但是该增益受到 AGL DRC 的门限限制。

Table 10. Analog Gain Setting

AGAIN(4:0)	GAIN (dBFS)	AMPLIFIER PEAK OUTPUT VOLTAGE (V)
00000	0	29.5
00001	–0.5	27.85
…	…	…
11111	–15.5	4.95

8.4 器件功能模式

8.4.1 软件控制

AU6815E 通过 I²C 通信接口进行配置，最高支持 400kHz I²C。详情请参考 I²C SERIAL COMMUNICATION BUS 章节。

- BTL mode
- PBTL mode

8.4.1.1 BTL MODE

在 BTL 模式下，输出两路独立，分别为左声道输出和右声道输出。在信号链上看，这两路从输入、DSP 算法处理和输出都支持独立配置。AU6815E 支持单独关闭一个通道，让另外一个通道正常工作。

8.4.1.2 PBTL MODE

AU6815E 还可以支持 PBTL 模式(两个 BTL 模式进行并联)。在 PBTL 模式下，输出功率和输出最大电流都可以翻倍。此外，电路图上支持电感前并联或者电感后的并联，这个取决于设计峰值电流和电感饱和电流及成本之间的平衡。在驱动大功率低音炮时，通常会选择 PBTL 模式。在该模式下，信号链上一般默认选择左声道为 PBTL 输出。

8.4.2 芯片状态控制

AU6815E 主要有 5 种模式：

1. Shutdown: 在$\overline{\text{PDN}}$拉低后，内部 LDO 都会关闭，此时功耗最低。
2. Deep Sleep: I²C 正常通讯、数字核的供电正常、模拟部分 LDO 关闭、DSP 处于活动状态。
3. Sleep: I²C 模块、数字核、DSP 均正常工作。此外，模拟部分 5V Analog LDO 正常工作。
4. Output Hi-Z: 除了输出 power stage 外，都处于 active 状态。
5. Play: 当 register 0x03h-D(1:0) = 11，器件工作在 Play 模式。

8.4.3 芯片调制模式

AU6815E 支持 BD 调制模式和 1SPW 调制模式。

8.4.3.1 BD 调制模式

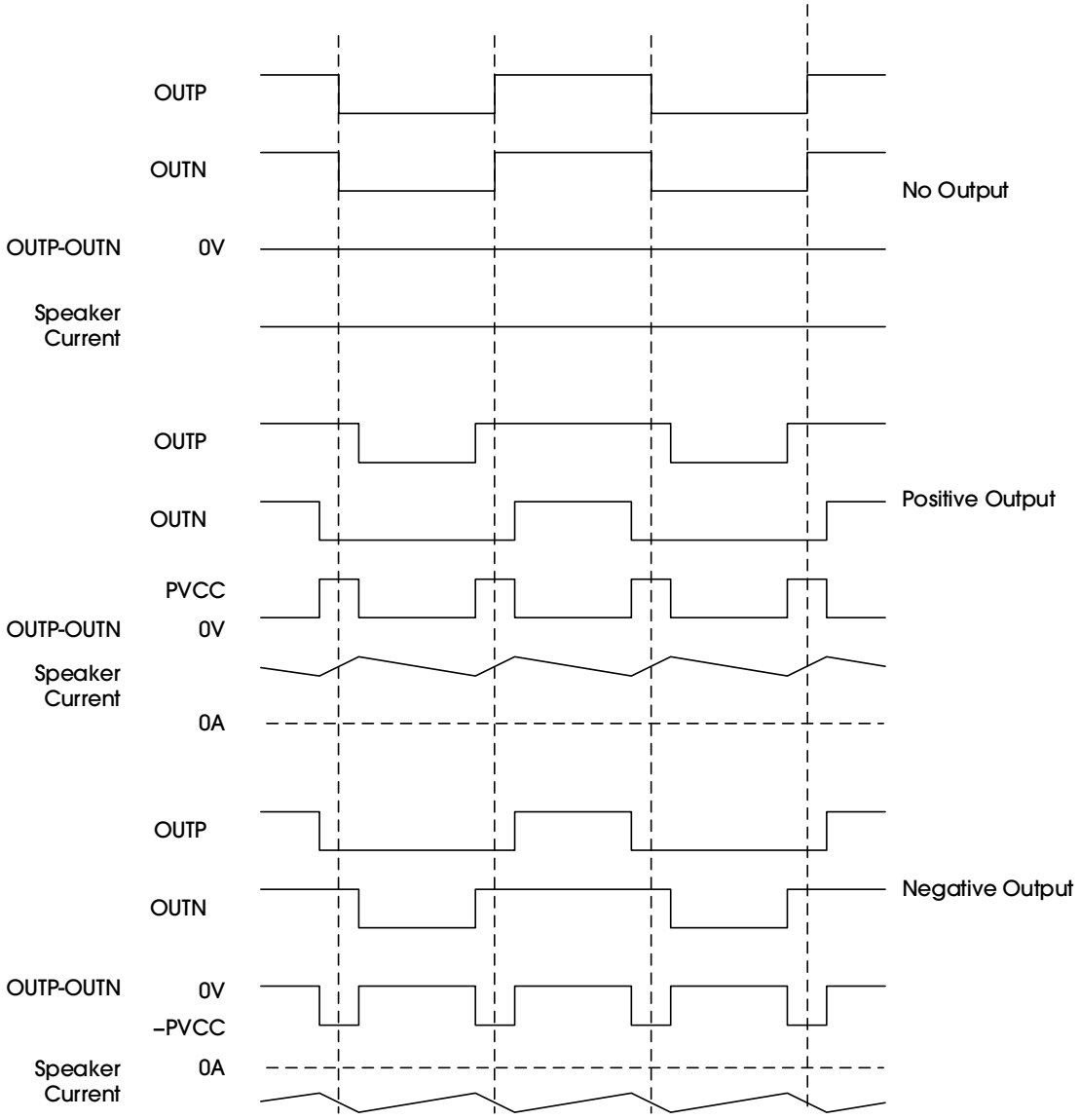


Figure 25. BD Mode Modulation

8.4.3.2 1SPW 调制模式

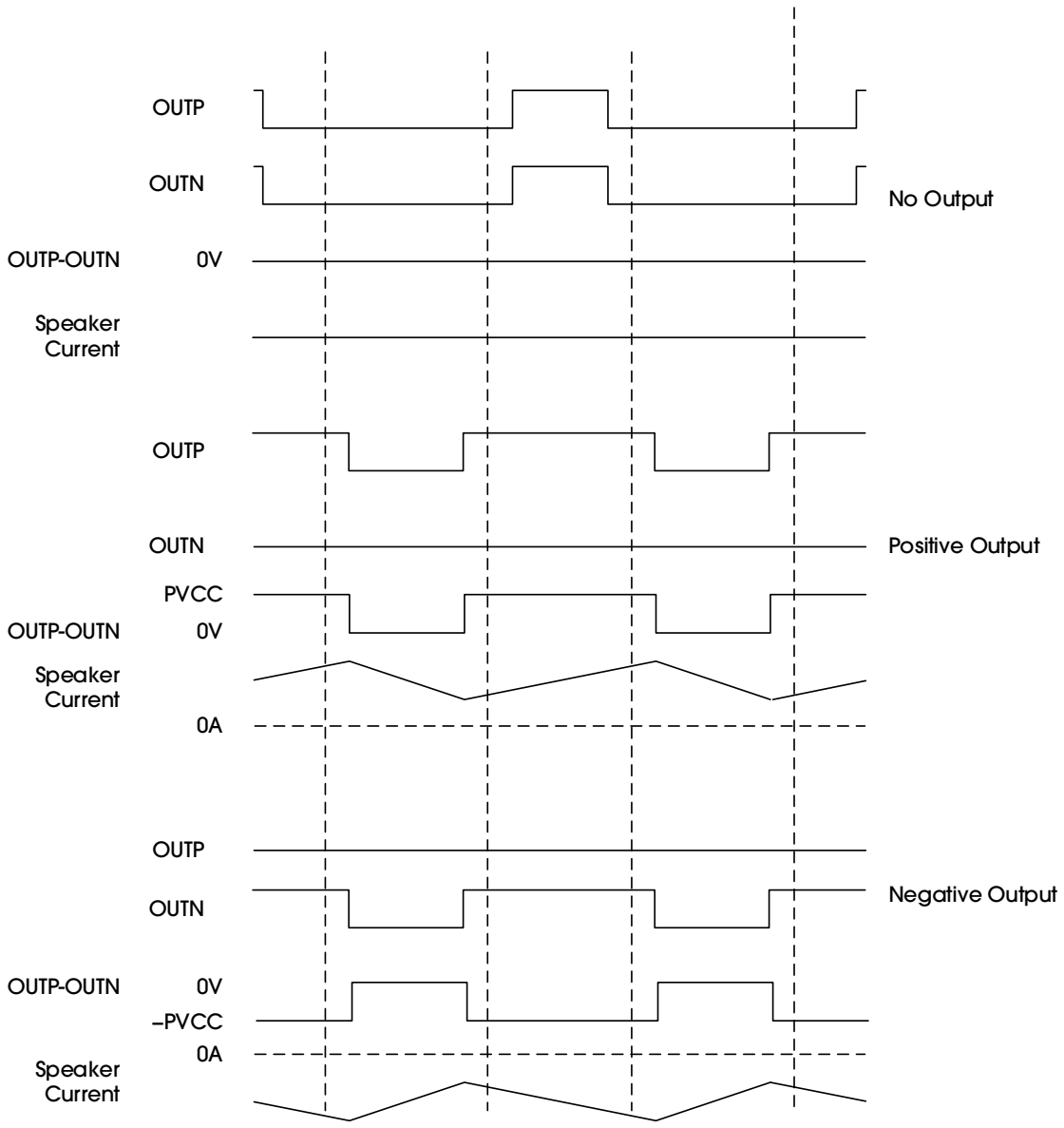


Figure 26. 1SPW Mode Modulation

8.5 编程和控制

8.5.1 I²C 通讯总线

AU6815E 支持标准或者 fast I²C，标称寻址方式分为 book、page 和 register 的架构。

8.5.2 从机地址

从机地址通过 ADR 管脚进行配置，具体如 Table 11 所示。

Table 11. I²C Slave Address Configuration

ADR PIN CONFIGURATION	MSB					USER-DEFINED		LSB
4.7kΩ to DVDD	0	1	0	1	1	0	0	R/$\overline{W}$
15kΩ to DVDD	0	1	0	1	1	0	1	R/$\overline{W}$
47kΩ to DVDD	0	1	0	1	1	1	0	R/$\overline{W}$
120kΩ to DVDD	0	1	0	1	1	1	1	R/$\overline{W}$

8.5.2.1 随机写入

随机写入格式如下：

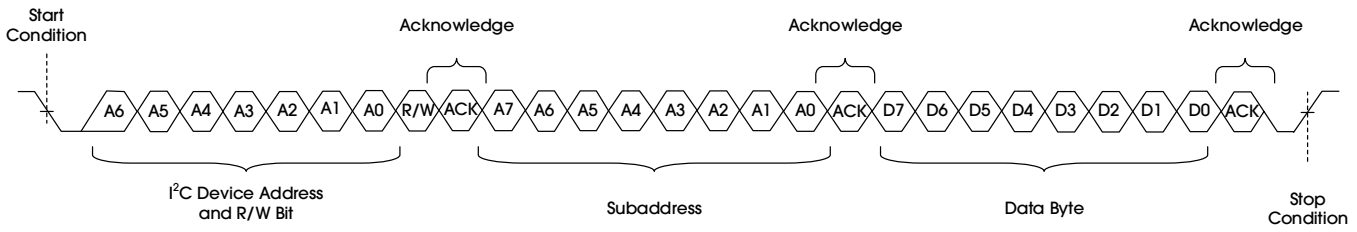


Figure 27. Random Write Transfer

8.5.2.2 顺序写入

顺序写入格式如下：

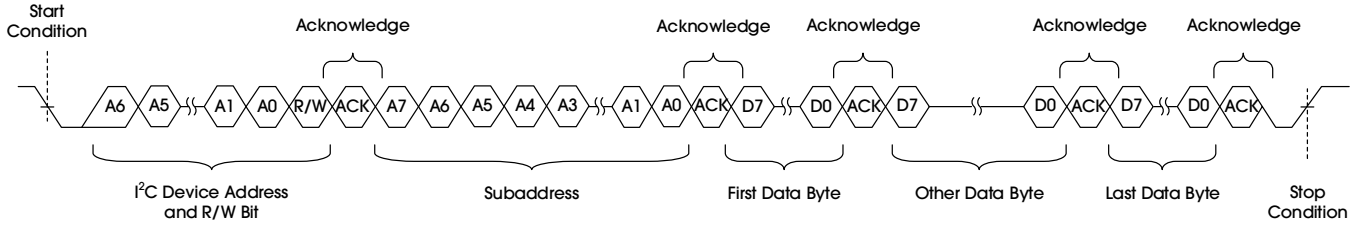


Figure 28. Sequential Write Transfer

8.5.2.3 随机读取

随机读取如下：

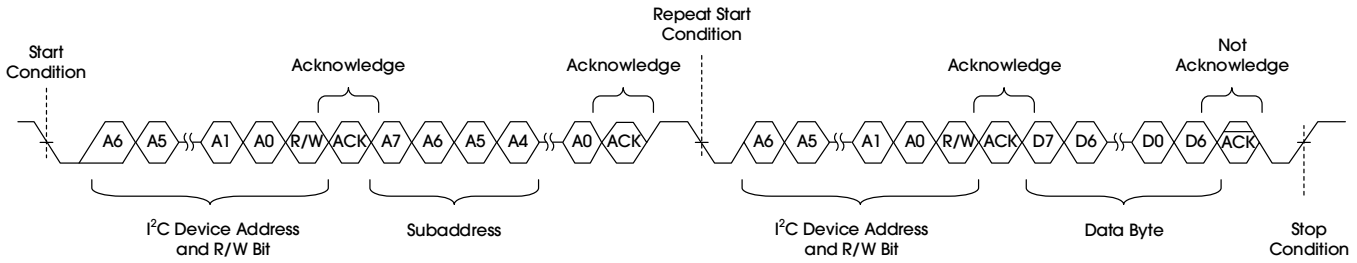


Figure 29. Random Read Transfer

8.5.2.4 顺序读取

顺序读取时序如下：

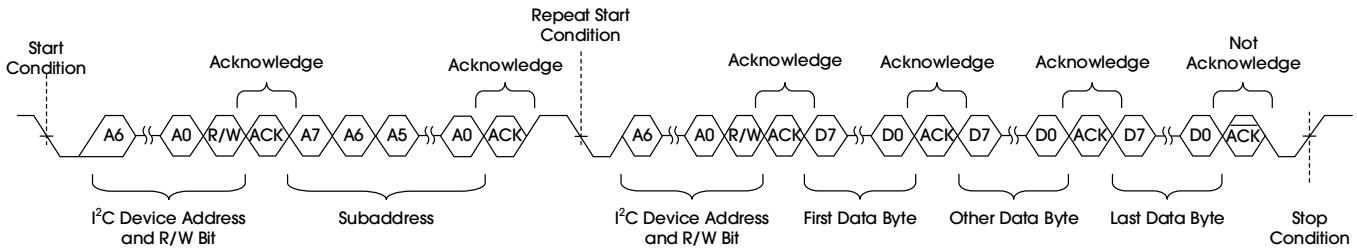


Figure 30. Sequential Read Transfer

8.5.2.5 内存空间结构及参数更新

AU6815E book 操作通过 0x7f 进入相应的 book，通过 0x00 进入相应的 page。每次切换 book，需要先进入 Page 0。每次新进入一个 book，默认进入 Page 0。

8.5.3 软件控制

8.5.3.1 上电时序

1. 配置 ADR/$\overline{FAULT}$设置 I²C 地址。
2. PVDD 和 DVDD 上电。PVDD 和 DVDD 无上电时序先后要求。
3. PVDD 和 DVDD 上电完成 1ms 后，拉高$\overline{PDN}$。
4. $\overline{PDN}$拉高后等待 1ms，然后配置 I²C 进入 play。I²C 配置过程中间无需插入延迟时间，且不需要 I²S 时钟存在。

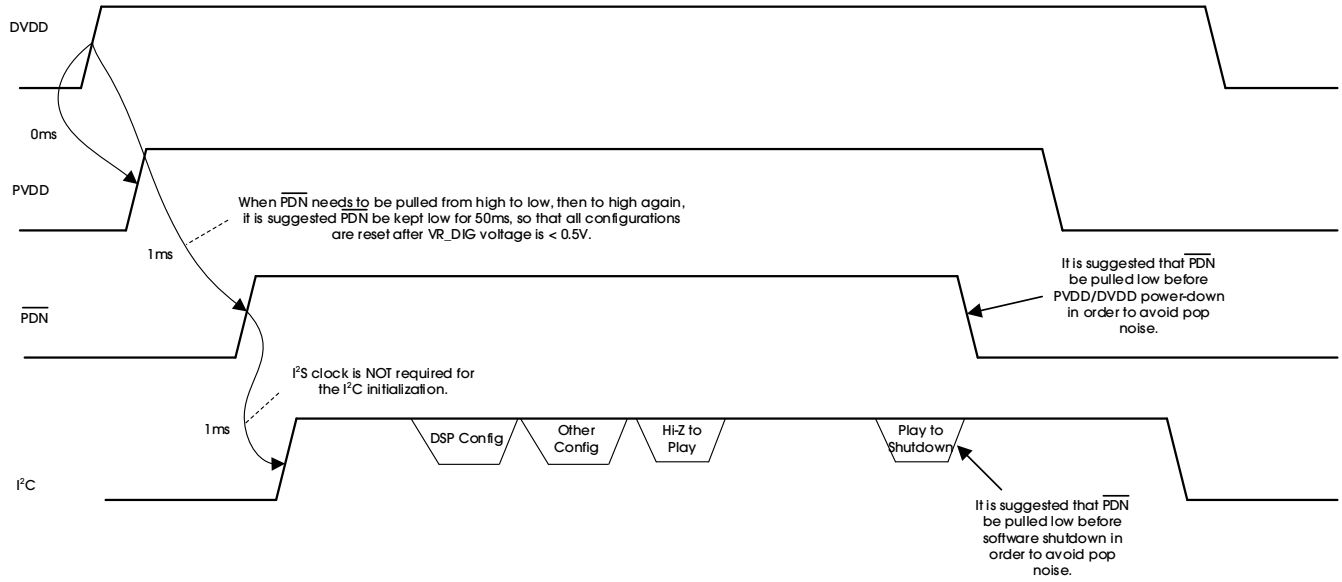


Figure 31. Start-up and Power-Down Sequence

8.5.3.2 下电时序

1. 芯片正常工作
2. 配置寄存器让芯片进入 Hi-Z 或以下的状态，然后拉低$\overline{PDN}$
3. 等待 10ms
4. 拉低 PVDD，再拉低 DVDD
5. 芯片处于下电状态

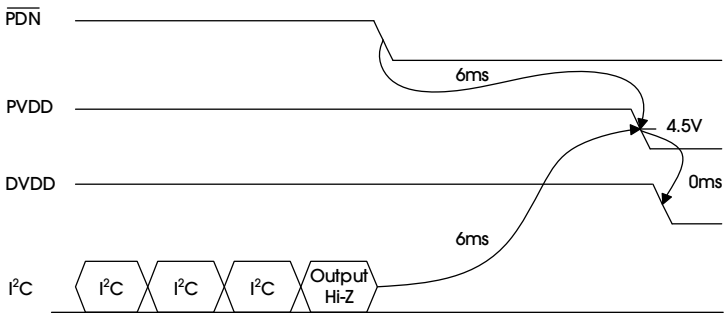


Figure 32. Power-Down Sequence

在 PVDD 和 DVDD 掉电之前，建议提前至少 6ms 软件关闭输出，比如在进入 Hi-Z 模式之后拉低$\overline{PDN}$，这样可以有效的避免掉电 pop 音。

8.5.3.3 保护和监测

8.5.3.3.1 过流关断保护(OCSD)

在严重短路事件(例如输出短路到 PVDD 或 GND，或者喇叭短路)下，可能会导致输出两个通道任一通道存在瞬时大电流，如果该瞬时大电流超过芯片过流保护门限，则芯片将会在 100ns 内关闭芯片两个通道。过流关断速度取决于多种因素，例如短路阻抗、电源电压和开关频率，触发过流保护后，芯片不会自动重启，用户可以通过 I^2C 重新启动芯片进入工作状态。OCSD 事件会激活故障引脚，并且 I^2C 故障寄存器会保存事件发生记录。

8.5.3.3.2 扬声器直流保护

如果芯片输出级电压存在大于 1.9V (Typ)的直流偏移电压，并且持续超过 600ms (Typ)，$\overline{\text{FAULT}}$引脚会被触发拉低并且导致芯片两路输出关闭进入 Hi-Z 状态，该错误状态也会记录在 Book0/Page0 中的寄存器 0x70 中，且该错误状态不会自动恢复，需要软件手动配置 0x0D 寄存器清除 fault 后，才可以重新进入播放状态。

8.5.3.3.3 器件过热保护

一旦芯片温度超过 160°C (Typ)，器件会将输出驱动器从播放模式设置为高阻抗模式。 Book0/Page0 中的寄存器 0x72 报告过温关机故障。此故障的行为设置为自动恢复模式，一旦芯片温度降至 150°C，器件将自动返回播放模式，用户也可以通过清除 Book0/Page0 中的寄存器 0x0D 的故障记录来重新进入播放模式。

8.5.3.3.4 过压保护和欠压保护

8.5.3.3.4.1 过压保护

一旦 PVDD 电压超过过压保护门限 (典型值 28V)，芯片将从播放模式进入 Hi-Z 模式，并且 Book0/Page0 中的寄存器 0x71 报告过压故障。一旦 PVDD 降至 28V (典型值)以下，芯片将返回播放模式。但是寄存报错记录需要通过 Book0/Page0 中的寄存器 0xOD 清除，否则该错误标志位仍保持为 1。

8.5.3.3.4.2 欠压保护

一旦 PVDD 电压降至欠压保护门限 (典型值 4.2V)以下，芯片将从播放模式进入 Hi-Z 模式，并且 Book0/Page0 中的寄存器 0x71 报告过压故障。一旦 PVDD 升高至 4.2V (典型值)以上，芯片将返回播放模式。但是寄存报错记录需要通过 Book0/Page0 中的寄存器 0xOD 清除，否则该错误标志位仍保持为 1。

8.5.3.3.5 I^2S 时钟错误

时钟一般是由于外部输入的 I^2S 时钟发生 Clock 信号停止、SCLK/LRCLK 比例错误、LRCLK 时钟频率不符合标准等情况导致。芯片的 Book0/Page0 寄存器 0x37 和寄存器 0x39 会实时监测时钟状态，如果有错，会通过寄存器 0x71 报出。发生时钟错误时，芯片默认进入 sleep 状态，也可以通过寄存器，从而实现低功耗。Clock fault 可以在寄存器 0x71 中读取。

9. REGISTER MAPS

Table 12 lists the memory-mapped registers for the control port. All register offset addresses not listed in Table 12 should be considered as reserved locations and the register contents should not be modified.

Table 12. Control Port Registers

OFFSET	ACRONYM	REGISTER NAME
1h	RESET_CTRL	Register 1
2h	DEVICE_CTRL_1	Register 2
3h	DEVICE_CTRL_2	Register 3
4h	POWER STATE	Register 4
Dh	RESET_CTRL_2	Register 13
Fh	I2C_PAGE_AUTO_INC	Register 15
28h	SIG_CH_CTRL	Register 40
29h	CLOCK_DET_CTRL	Register 41
30h	SDOUT_SEL	Register 48
31h	I2S_CTRL	Register 49
33h	SAP_CTRL1	Register 51
34h	SAP_CTRL2	Register 52
35h	SAP_CTRL3	Register 53
37h	FS_MON	Register 55
38h	BCK_MON	Register 56
39h	CLKDET_STATUS	Register 57
4Ch	DIG_VOL_LEFT	Register 76
4Dh	DIG_VOL_RIGHT	Register 77
4Eh	DIG_VOL_CTRL2	Register 78
4Fh	DIG_VOL_CTRL3	Register 79
53h	ANA_CTRL	Register 83
54h	AGAIN	Register 84
5Ch	BQ_WR_CTRL1	Register 92
62h	GPIO0/ADR	Register 98
63h	GPIO1	Register 99
64h	GPIO2	Register 100
67h	DIE_ID	Register 105
6Ah	PHASE_CTRL	Register 108
70h	CHAN_FAULT	Register 112
71h	GLOBAL_FAULT1	Register 113
72h	WARNING1	Register 114
73h	WARNING2	Register 115
74h	PIN_CONTROL1	Register 116
75h	PIN_CONTROL2	Register 117
76h	MISC_CONTROL	Register 118

Complex bit access types are encoded to fit into small table cells. Table 13 shows the codes that are used for access types in this section.

Table 13. Control Port Access Type Codes

ACCESS TYPE	CODE	DESCRIPTION
READ TYPE		
R	R	Read
WRITE TYPE		
W	W	Write
RESETOR DEFAULT VALUE		
-n		Value after reset or the default value

9.1 RESET_CTRL REGISTER (OFFSET = 1H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 14. RESET_CTRL Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:5	RESERVED	R	000	Reserved
4	RST_MOD	W	0	WRITE CLEAR BIT Reset modules This bit resets the interpolation filter and the DAC modules. Since the DSP is also reset, the coefficient RAM content will also be cleared by the DSP. This bit is auto cleared and can be set only in the Hi-Z mode. 0: Normal 1: Reset modules
3:1	RESERVED	R	000	Reserved
0	RST_REG	W	0	Write clear bit Reset registers This bit resets the mode registers back to their initial values. The RAM content is not cleared. This bit is auto cleared and must be set only when the DAC is in the Hi-Z mode (resetting registers when the DAC running is prohibited and not supported). 0: Normal 1: Reset the mode registers

9.2 DEVICE_CTRL_1 REGISTER (OFFSET = 2H) [RESET = 0X50]

Return to SUMMARY TABLE.

Table 15. DEVICE_CTRL_1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	RESERVED	R	0	Reserved
6:4	FSW_SEL	R/W	5	Select F_{SW} (kHz) 0: 260 1: 310 2: 384 3: 480 4: 576 5: 768 Others: Reserved
3	RESERVED	R	0	Reserved
2	DAMP_PBTL	R/W	0	0: Set DAMP to the BTL mode 1: Set DAMP to the PBTL mode
1:0	DAMP_MOD	R/W	00	00: BD mode 01: 1SPW mode Others: Reserved

9.3 DEVICE_CTRL_2 REGISTER (OFFSET = 3H) [RESET = 0X10]

Return to SUMMARY TABLE.

Table 16. DEVICE_CTRL_2 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	RESERVED	R	0	Reserved
6	DEEPSLEEP_ON_CLKF	R/W	0	Power state goes to the deep sleep mode when I2S clock fault happens.
5	RESERVED	R	0	Reserved
4	DIS_DSP	R/W	1	DSP reset 0: Normal operation 1: Reset the DSP
3	MUTE	R/W	0	Mute left/right channel This bit issues soft mute request for the left/right channel. The volume will be smoothly ramped down/up to avoid pop/click noise. 0: Normal volume 1: Mute
2	RESERVED	R	0	Reserved
1:0	CTRL_STATE	R/W	00	Device state control register 00: Deep Sleep 01: Sleep 10: Hi-Z 11: Play

9.4 POWER STATE REPORT (OFFSET = 4H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 17. Power State Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:2	RESERVED	R	0	Reserved
1:0	Power State Report	R	0	Power state report 00: Deep Sleep 01: Sleep 10: Hi-Z 11: Play

9.5 RESET_CTRL_2 REGISTER (OFFSET = DH) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 18. RESET_CTRL_2 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	SYNC_FLAG	R/W	0	0: Sync is not done. 1: Sync is properly done.
6:1	RESERVED	R	0	Reserved.
0	CTRL_STATE	W	0	1: Clear analog fault

9.6 I2C_PAGE_AUTO_INC REGISTER (OFFSET = FH) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 19. I2C_PAGE_AUTO_INC Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:4	RESERVED	R	0000	Reserved
3	PAGE_AUTOINC_DIS	R/W	0	Page auto increment disable Disable page auto increment mode for non-zero books. When end of page is reached, it goes back to the 8th address location of next page when this bit is 0. When this bit is 1, it goes to the 0th location of current page itself like in older part. 0: Enable Page auto increment 1: Disable Page auto increment
2:0	RESERVED	R	000	Reserved

9.7 SIG_CH_CTRL REGISTER (OFFSET = 28H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 20. SIG_CH_CTRL Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:4	BCK_RATIO_CONFIGURE	R/W	0000	Configured BCK ratio—the number of BCK clocks in one audio frame 0011: 32FS 0101: 64FS 0111: 128FS 1001: 256FS 1011: 512FS
3:0	FS_CFG	R/W	0000	FS speed mode These bits select the FS operation mode, which must be set according to the current audio sampling rate. 4'b0000: Auto detection 4'b0110: 32kHz 4'b1000: 44.1kHz 4'b1001: 48kHz 4'b1010: 88.2kHz 4'b1011: 96kHz Others: Reserved

9.8 CLOCK_DET_CTRL REGISTER (OFFSET = 29H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 21. CLOCK_DET_CTRL Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	RESERVED	R	0	Reserved
6	DIS_DET_PLL	R/W	0	Ignore PLL underrate/overate detection This bit controls whether to ignore the PLL underrate/overrate detection. The PLL clock must be faster than 10MHz otherwise error will be reported. The PLL must be slower than 150MHz otherwise an error will be reported. When ignored, a PLL underrate/overrate error will not cause a clock error. 0: Regard PLL underrate/overrate detection 1: Ignore PLL underrate/overrate detection
5	DIS_DET_BCLK_RANGE	R/W	0	Ignore BCK range detection This bit controls whether to ignore the BCK range detection. The BCK must be stable between 256kHz and 50MHz otherwise an error will be reported. When ignored, a BCK range error will not cause a clock error. 0: Regard BCK range detection 1: Ignore BCK range detection
4	DIS_DET_FS	R/W	0	Ignore FS error detection This bit controls whether to ignore the FS error detection. When ignored, FS error will not cause a clock error, however, CLKDET_STATUS will report FS error. 0: Regard FS detection 1: Ignore FS detection
3	DIS_DET_BCLK	R/W	0	Ignore BCK detection This bit controls whether to ignore the BCK detection against LRCK. The BCK must be stable between 32FS and 512FS inclusive otherwise an error will be reported. When ignored, a BCK error will not cause a clock error. 0: Regard BCK detection 1: Ignore BCK detection
2	DIS_DET_MISS	R/W	0	Ignore BCK missing detection This bit controls whether to ignore the BCK missing detection. When ignored, a BCK missing will not cause a clock error. 0: Regard BCK missing detection 1: Ignore BCK missing detection
1:0	RESERVED	R	0	Reserved

9.9 SDOUT_SEL REGISTER (OFFSET = 30H) [RESET = 0H]

Return to SUMMARY TABLE.

Table 22. SDOUT_SEL Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:1	RESERVED	R	0	Reserved
0	SDOUT_SEL	R/W	0	Sdout select 0: SDOUT is the DSP output (post-processing). 1: SDOUT is the DSP input (pre-processing).

9.10 I2S_CTRL REGISTER (OFFSET = 31H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 23. I2S_CTRL Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	RESERVED	R	00	Reserved
5	BCK_INV	R/W	0	BCK polarity This bit sets the inverted BCK mode. In the inverted BCK mode, the DAC assumes that the LRCK and DIN edges are aligned to the rising edge of the BCK. Normally they are assumed to be aligned to the falling edge of the BCK. 0: Normal BCK mode 1: Inverted BCK mode
4:0	RESERVED	R	00000	Reserved

9.11 SAP_CTRL1 REGISTER (OFFSET = 33H) [RESET = 0X02]

Return to SUMMARY TABLE.

Table 24. SAP_CTRL1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	I2S_SHIFT_MSB	R/W	0	I^2S shift MSB
6	RESERVED	R	0	Reserved
5:4	DATA_FORMAT	R/W	00	I^2S data format These bits control both input and output audio interface formats for DAC operation. 00: I^2S 01: TDM/DSP 10: RTJ 11: LTJ
3:2	I2S_LRCLK_PULSE	R/W	00	01: LRCLK pulse < 8 SCLK. If the high width of LRCLK/FS in the TDM/DSP mode is less than 8 cycles of SCK, these two bits need set to 01.
1:0	WORD_LENGTH	R/W	10	I^2S word length These bits control both input and output audio interface sample word lengths for DAC operation. 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits

9.12 SAP_CTRL2 REGISTER (OFFSET = 34H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 25. SAP_CTRL2 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:0	I2S_SHIFT	R/W	00000000	I^2S shift LSB These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of BCK from the starting (MSB) of audio frame to the starting of the desired audio sample. 000000000: Offset = 0 BCK (no offset) 000000001: Offset = 1 BCK 000000010: Offset = 2 BCKs … 111111111: Offset = 511 BCKs

9.13 SAP_CTRL3 REGISTER (OFFSET = 35H) [RESET = 0X11]

Return to SUMMARY TABLE.

Table 26. SAP_CTRL3 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	RESERVED	R	00	Reserved
5:4	LEFT_DAC_DPATH	R/W	01	Left DAC data path These bits control the left channel audio data path connection. 00: Zero data (mute) 01: Left channel data 10: Right channel data 11: Reserved (do not set)
3:2	RESERVED	R	00	Reserved
1:0	RIGHT_DAC_DPATH	R/W	01	Right DAC data path These bits control the right channel audio data path connection. 00: Zero data (mute) 01: Right channel data 10: Left channel data 11: Reserved (do not set)

9.14 FS_MON REGISTER (OFFSET = 37H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 27. FS_MON Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	RESERVED	R	00	Reserved
5:4	BCLK_RATIO_HIGH	R	00	2 MSBs of the detected BCK ratio
3:0	FS_RPT	R	0000	Currently detected audio sampling rate 4'b0000: FS Error 4'b0110: 32kHz 4'b1000: Reserved 4'b1001: 48kHz 4'b1011: 96kHz Others: Reserved

9.15 BCK_MON REGISTER (OFFSET = 38H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 28. BCK_MON Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:0	BCLK_RATIO_LSB	R	00000000	Currently detected BCK ratio—number of BCK clocks in one audio frame BCK = 32FS to 512FS

9.16 CLKDET_STATUS REGISTER (OFFSET = 39H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 29. CLKDET_STATUS Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	RESERVED	R	00	Reserved
5	BCK_OVR_UNR	R	0	This bit indicates whether the BCLK is overrated or underrated.
4	PCLK_OVR_UNR	R	0	This bit indicates whether the PLL is overrated or underrated.
3	PLL_LOCK	R	0	This bit indicates whether the PLL is locked. The PLL will be reported as unlocked when it is disabled.
2	BCLK_HALT	R	0	This bit indicates whether the BCK is missing.
1	BCLK_RATIO_ERR	R	0	This bit indicates whether the BCK is valid. The BCK ratio must be stable and in the range of 32FS-512FS to be valid.
0	FS_ERR	R	0	In the auto detection mode (reg_fs_cfg = 0), this bit indicates whether the audio sampling rate is valid. In non-auto detection mode (reg_fs_cfg ≠ 0), FS error indicates that the configured FS is different from the detected FS. Even FS Error Detection Ignore is set, this flag will also be asserted.

9.17 DIG_VOL_LEFT REGISTER (OFFSET = 4CH) [RESET = 30H]

Return to SUMMARY TABLE.

Table 30. DIG_VOL_CTR Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:0	PGA_LEFT	R/W	00110000	Left digital volume These bits control the left channel digital volume. The digital volume is 24dB to –103dB in steps of –0.5dB. 00000000: +24.0dB 00000001: +23.5dB … 00101111: +0.5dB 00110000: 0.0dB 00110001: –0.5dB … 11111110: –103dB 11111111: Mute

9.18 DIG_VOL_RIGHT REGISTER (OFFSET = 4DH) [RESET = 30H]

Return to SUMMARY TABLE.

Table 31. DIG_VOL_CTR Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:0	PGA_RIGHT	R/W	00110000	Right digital volume These bits control the left channel digital volume. The digital volume is 24dB to –103dB in steps of –0.5dB. 00000000: +24.0dB 00000001: +23.5dB … 00101111: +0.5dB 00110000: 0.0dB 00110001: –0.5dB ... 11111110: –103dB 11111111: Mute

9.19 DIG_VOL_CTRL2 REGISTER (OFFSET = 4EH) [RESET = 0X33]

Return to SUMMARY TABLE.

Table 32. DIG_VOL_CTRL2 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	PGA_RAMP_DOWN_SPEED	R/W	00	Digital volume normal ramp down frequency These bits control the frequency of the digital volume updates when the volume is ramping down. The setting here is applied to the soft mute request. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (instant mute)
5:4	PGA_RAMP_DOWN_STEP	R/W	11	Digital volume normal ramp down step These bits control the step of the digital volume updates when the volume is ramping down. The setting here is applied to the soft mute request. 00: Decrement by 4dB for each update 01: Decrement by 2dB for each update 10: Decrement by 1dB for each update 11: Decrement by 0.5dB for each update
3:2	PGA_RAMP_UP_SPEED	R/W	00	Digital volume normal ramp up frequency These bits control the frequency of the digital volume updates when the volume is ramping up. The setting here is applied to the soft unmute request. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly restore the volume (instant unmute)
1:0	PGA_RAMP_UP_STEP	R/W	11	Digital volume normal ramp up step These bits control the step of the digital volume updates when the volume is ramping up. The setting here is applied to the soft unmute request. 00: Increment by 4dB for each update 01: Increment by 2dB for each update 10: Increment by 1dB for each update 11: Increment by 0.5dB for each update

9.20 DIG_VOL_CTRL3 REGISTER (OFFSET = 4FH) [RESET = 0X30]

Return to SUMMARY TABLE.

Table 33. DIG_VOL_CTRL3 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	FAST_RAMP_DOWN_SPEED	R/W	00	Digital volume emergency ramp down frequency These bits control the frequency of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared with normal soft mute. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (instant mute)
5:4	FAST_RAMP_DOWN_STEP	R/W	11	Digital volume emergency ramp down step These bits control the step of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute. 00: Decrement by 4dB for each update 01: Decrement by 2dB for each update 10: Decrement by 1dB for each update 11: Decrement by 0.5dB for each update
3:0	RESERVED	R	0000	Reserved

9.21 ANA_CTRL REGISTER (OFFSET = 53H) [RESET = 0X49]

Return to SUMMARY TABLE.

Table 34. ANA_CTRL Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:0	Bandwidth	R/W	0x49	Bandwidth depends on F_{SW} BD mode: F_{SW} = 260kHz (0xD4) F_{SW} = 310kHz (0xB4) F_{SW} = 384kHz (0x94) F_{SW} = 480kHz (0x84) F_{SW} = 576kHz (0x64) F_{SW} = 768kHz (0x44) 1SPW mode: F_{SW} = 260kHz (0xE8) F_{SW} = 310kHz (0xC8) F_{SW} = 384kHz (0x88) F_{SW} = 480kHz (0xA4) F_{SW} = 576kHz (0x88) F_{SW} = 768kHz (0x64)

9.22 AGAIN REGISTER (OFFSET = 54H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 35. AGAIN Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:5	RESERVED	R	000	Reserved
4:0	ANA_GAIN	R/W	00000	Analog gain control This bit controls the channel analog gain. 00000: 0dB 00001: –0.5dB … 11111: –15.5dB

9.23 BQ_WR_CTRL1 REGISTER (OFFSET = 5CH) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 36. BQ_WR_CTRL1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:1	RESERVED	R	0000000	Reserved
0	BQ_WR_FIRST_COEF	R/W	0	Indicate the first coefficient of a BQ is starting to write.

9.24 GPIO0/ADR REGISTER (OFFSET = 62H) [RESET = 2EH]

Return to SUMMARY TABLE.

Table 37. GPIO0_ADR Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:5	Reserved	R	1h	Reserved
4:0	GPIO0	R/W	0Eh	01000: Open drain output as fault warning; 01001: Open drain output as clock invalid 11010: As PVDD drop flag 01110: Open drain output as fault Others: Reserved

9.25 GPIO1 REGISTER (OFFSET = 63H) [RESET = 00H]

Return to SUMMARY TABLE.

Table 38. GPIO1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	Reserved	R	0h	Reserved
5	ADR_Dir	R/W	0h	1: GPIO as output 0: GPIO as input
4:0	GPIO1	R/W	0h	00011: Digital input as Hi-Z 01000: Open drain output as fault warning; 01100: Sdout 01110: As fault pin 11001: Digital input as mute … Others: Reserved

9.26 GPIO2 REGISTER (OFFSET = 64H) [RESET = 2CH]

Return to SUMMARY TABLE.

Table 39. GPIO2 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	Reserved	R	0	Reserved
5	ADR_Dir	R/W	1h	1: GPIO as output 0: GPIO as input
4:0	GPIO2	R/W	0Ch	00011: Digital input as Hi-Z 01000: Open drain output as fault warning; 01100: Sdout 01110: As fault pin 11001: Digital input as mute … Others: Reserved

9.27 DIE_ID REGISTER (OFFSET = 67H) [RESET = 90H]

Return to SUMMARY TABLE.

Table 40. DIE_ID Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:0	DIE_ID	RO	10010000	Die ID of the device

9.28 PHASE_CTRL REGISTER (OFFSET = 6AH) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 41. PHASE_CTR Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:4	SYNC_MODE	R/W	0000	Synch mode 4'h0: No phase sync 4'hD: GPI phase sync 4'hE: Reg phase sync 4'hF: LRCLK phase sync
3	RAMP_PHASE_SEL	R/W	00	Channel 2 phase selection 0: ph_ch2 = ph_ch1 + 180 deg 1: ph_ch2 = ph_ch1
2:0	I2S_SYNC_EN	R/W	000	Select ramp clock phase when multi devices integrated in one system to reduce EMI and peak supply peak current, it is recommended set all devices the same RAMP frequency and same spread spectrum. it must be set before driving device into PLAY mode if this feature is needed. Select the phase of Ch1: 0: 0 deg 1: 60 deg 2: 90 deg 3: 120 deg (intended for 3-chip cancellation) 4: 180 deg (intended for 2-chip cancellation) 5: 240 deg (intended for 3-chip cancellation) 6: 270 deg 7: 300 deg

9.29 CHAN_FAULT REGISTER (OFFSET = 70H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 42. CHAN_FAULT Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	RESERVED	R	00	Reserved
5	CBCF_CH2	R	0	Right channel cycle by cycle overcurrent fault
4	CBCF_CH1	R	0	Left channel cycle by cycle overcurrent fault
3	CH1_DC_1	R	0	Left channel DC fault
2	CH2_DC_1	R	0	Right channel DC fault
1	CH1_OC_I	R	0	Left channel overcurrent fault
0	CH2_OC_I	R	0	Right channel overcurrent fault

9.30 GLOBAL_FAULT1 REGISTER (OFFSET = 71H) [RESET = 0H]

Return to SUMMARY TABLE.

Table 43. GLOBAL_FAULT1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	OTP	R	0	1: Overtemperature error
6	Reserved	R	0	Reserved
5	OTP_UERR	R	0	1: OTP uncorrectable error
4	OTP_CERR	R	0	1: OTP correctable error
3	PDROP	R	0	1: PVDD drop
2	CLKF	R	0	1: Clock fault
1	POV	R	0	1: PVDD overvoltage fault
0	PUV	R	0	1: PVDD undervoltage fault

9.31 WARNING1 (OFFSET = 72H) [RESET = 0H]

Return to SUMMARY TABLE.

Table 44. WARNING1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	CLAMP_CH1	R	0	Left channel clamp warning
6	CLAMP_CH2	R	0	Right channel clamp warning
5:1	Reserved	R	00000	Reserved
0	OTSD_I	R	0	Overtemperature shutdown fault

9.32 WARNING2 (OFFSET = 73H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 45. OT_WARNING Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	CLIP_CH1	R	0	Left channel clip warning
6	CLIP_CH2	R	0	Right channel clip warning
5	CBCW_CH1	R	0	Left channel cycle by cycle overcurrent warning
4	CBCW_CH2	R	0	Right channel cycle by cycle overcurrent warning
3	OTW_LEVEL4	R	0	Overtemperature warning 146
2	OTW_LEVEL3	R	0	Overtemperature warning 135
1	OTW_LEVEL2	R	0	Overtemperature warning 125
0	OTW_LEVEL1	R	0	Overtemperature warning 113

9.33 PIN_CONTROL1 REGISTER (OFFSET = 74H) [RESET = 0X00]

Return to SUMMARY TABLE.

Table 46. PIN_CONTROL1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	MASK_OTF	R/W	0	Mask OTSD fault report
6	MASK_PDROP	R/W	0	Mask PVDD drop fault report
5	MASK_CLIP	R/W	0	Mask clip fault report
4	MASK_CLKF	R/W	0	Mask clock fault report
3	MASK_PUV	R/W	0	Mask PVDD UV fault report
2	MASK_POV	R/W	0	Mask PVDD OV fault report
1	MASK_DC	R/W	0	Mask DC fault report
0	MASK_OC	R/W	0	Mask OC fault report

9.34 PIN_CONTROL2 REGISTER (OFFSET = 75H) [RESET = 0X30]

Return to SUMMARY TABLE.

Table 47. PIN_CONTROL2 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	RESERVED	R	0	
6	LATCH_CBCW	R/W	0	1: Latch CBCW reported to warning
5	LATCH_CLKF	R/W	1	1: Latch CLKF reported to fault
4	LATCH_OTF	R/W	1	1: Latch OTSD reported to fault
3	LATCH_OTW	R/W	0	1: Latch OTW reported to warning
2	MASK_OTW	R/W	0	Mask OT warning report
1	MASK_CBCW	R/W	0	Mask CBC warning report
0	MASK_CBCF	R/W	0	Mask CBC fault report

9.35 MISC_CONTROL REGISTER (OFFSET = 76H) [RESET = 0XA1]

Return to SUMMARY TABLE.

Table 48. MISC_CONTROL Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	LATCH_CLKDET_2REG	R/W	1	1: Latch detailed clock detections reported to register map
6	LATCH_CLIP	R/W	0	1: Latch clip reported to warning
5	LATCH_PVDDF	R/W	1	1: Latch POV/PUV reported to fault
4	OTF_AUTOREC_EN	R/W	0	OTF auto recovery enable
3	LATCH_PDROP	R/W	0	1: Latch PDROP reported to fault
2	Reserved	R	0	Reserved
1	LATCH-CLAMP	R/W	0	Latches clamp reported to warning
0	MASK_CLAMP	R/W	1	Masks clamp reported to warning

10. 应用与实现

注
以下应用部分中的信息不是公司组件规范的一部分，公司不保证其准确性或完整性。公司的客户有责任确定组件是否适合他们的用途。客户应验证和测试他们的设计实施以确认系统功能。

10.1 自举电容

建议使用 0.22μF-0.47μF 的电容用于自举电容，通常建议使用 0.47μF。

10.1.1 电感选型

一般情况建议选择电感组合 10μH + 0.68μF 的组合，如果对静态电流有进一步要求，请参考如下建议。通常电感选型有四个关键参数：分别为电感感值、电感饱和电流、电感直流阻抗以及电感的线性度。首先电感值和饱和电流主要考虑如下几个公式：

1. 在输出启动瞬间，占空比会根据不同模式从 0 增加到 θ。

$$I_{peak\_power\_up} \approx PVDD \times \sqrt{C/L} \times \sin\left(1/\sqrt{L \times C} \times \theta / F_{SW}\right) \quad (1)$$

其中：

- θ = 0.5 (BD 模式)，或 0.14 (1SPW 模式)。

Equation 1 可以作为上电启动瞬间触发过流保护的选型参考，需要保证 $I_{peak\_power\_up}$ 低于过流保护门限。

Table 49. Peak Current during Power-Up

PVDD	L (μH)	C (μF)	F_{SW} (kHz)	$I_{peak\_power\_up}$
24	4.7	0.68	384	6.07A (> 5A OCP), not recommended
24	4.7	0.68	768	3.25A
24	10	0.68	384	3A
24	10	0.68	768	1.55A
12	4.7	0.68	384	3.32A
12	10	0.68	384	1.55A

2. 在播放模式下，音乐信号可能会导致输出削波，此时最坏情况引起最大电流为：

$$I_{peak\_clipping} \approx PVDD \times (1 - \theta) / (F_{SW} \times L) \quad (2)$$

3. 最大功率下流过电感电流为：

$$I_{peak\_output\_power} \approx \sqrt{2 \times Max\_Output\_Power / R_{Speaker\_Load}} \quad (3)$$

综合上述三个公式，建议电感饱和电流大于上述三个数值最大值，并且建议保留 30%左右的裕量。此外，最小感值建议如 Table 50 所示。

Table 50. LC Filter Recommendation

PVDD (V)	SWITCHING FREQUENCY (kHz)	MODULATION SCHEME	RECOMMENDED MINIMUM INDUCTANCE (μH) FOR LC FILTER DESIGN
≤ 12	384	BD	4.7μH + 0.68μF
> 12			10μH + 0.68μF
≤ 12	384	1SPW/Hybrid	10μH + 0.68μF
> 12			15μH + 0.68μF

如果选择更高的开关频率，建议最小感值大于等于 384kHz / F_{SW} × L。

10.1.2 供电去耦电容设计

推荐使用 0.1μF 电容用于高频滤波，且该电容应尽量靠近 PVDD。此外建议使用不小于 4 个 22μF 容量的电容用于去耦。

10.1.3 输出 EMI 滤波设计

出于 EMI 考虑，AU6815E 集成了高阶的展频配合硬件电路设计。详细参数设置，请联系类比支持。

10.2 典型应用

10.2.1 BTL 模式

Figure 33 展示了 AU6815E 工作在 BTL 模式下的原理图。

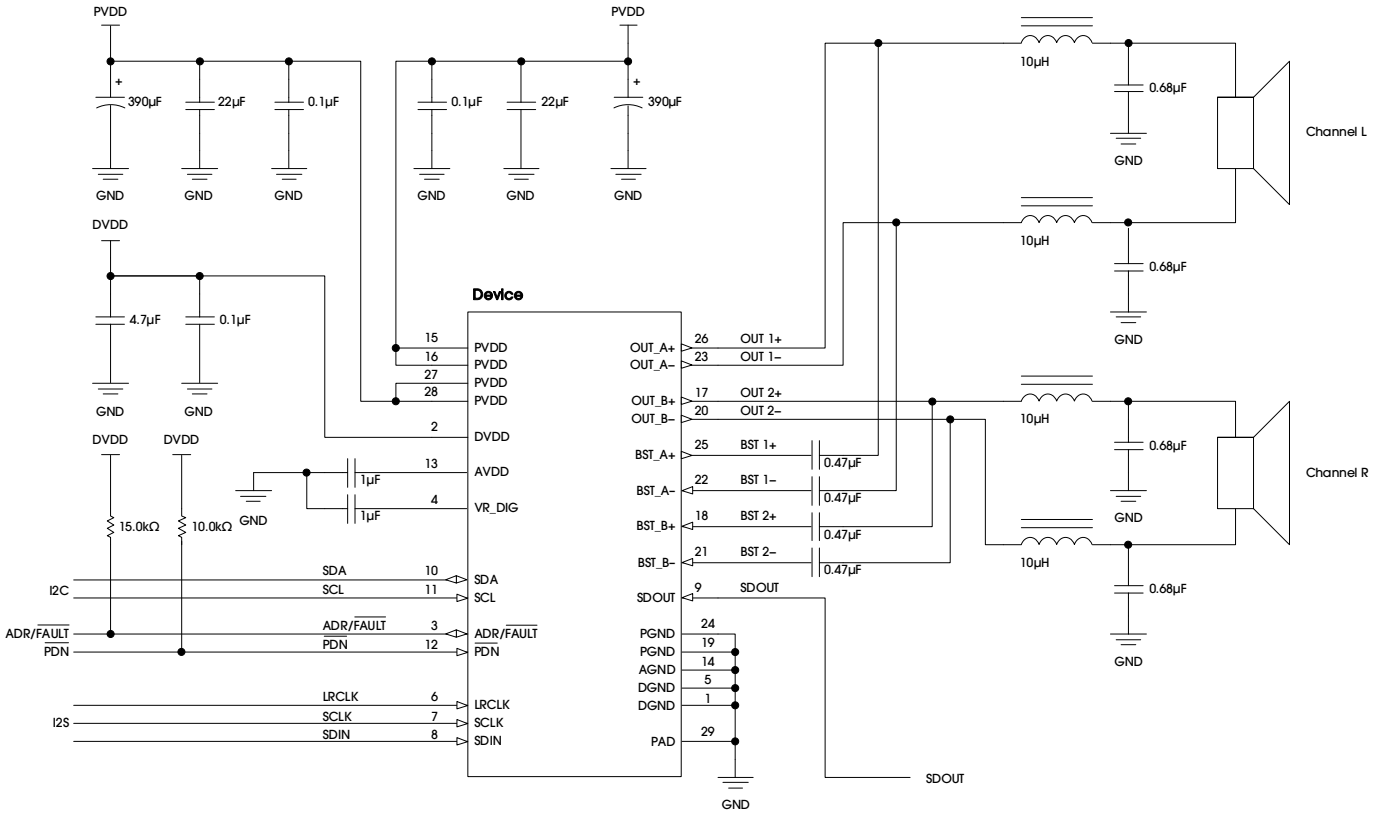


Figure 33. 2.0 (Stereo BTL) System Application Schematic

10.2.2 PBTL 模式

Figure 34 展示了 AU6815E 工作在 PBTL 模式下的原理图。

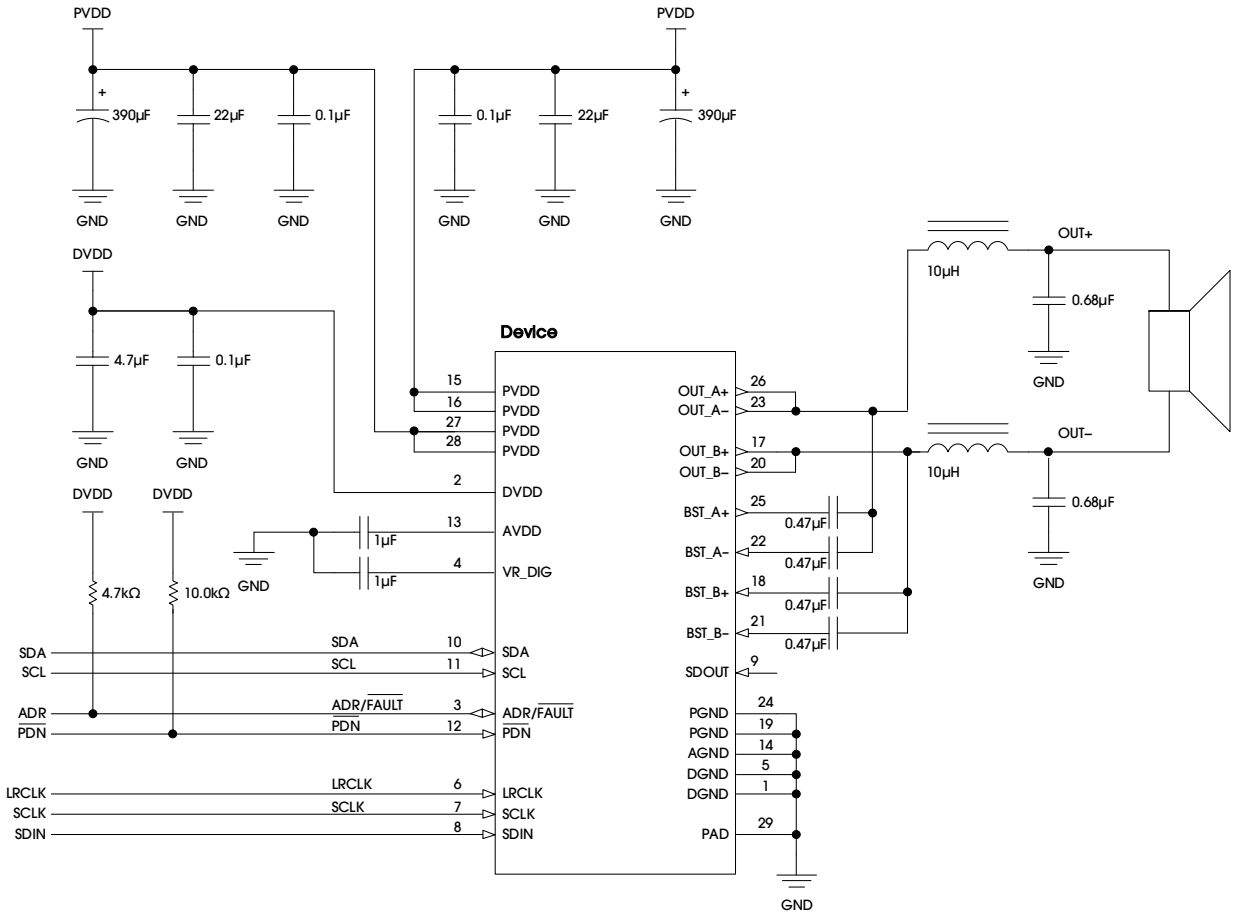


Figure 34. 1.0 (Mono PBTL) System Application Schematic

10.2.3 一站式调音软件平台

类比半导体提供一站式软件调试平台 ASATP。在该调试平台上输入调试参数，在评估板验证完毕后可以直接导出驱动配置头文件，方便客户软件集成。

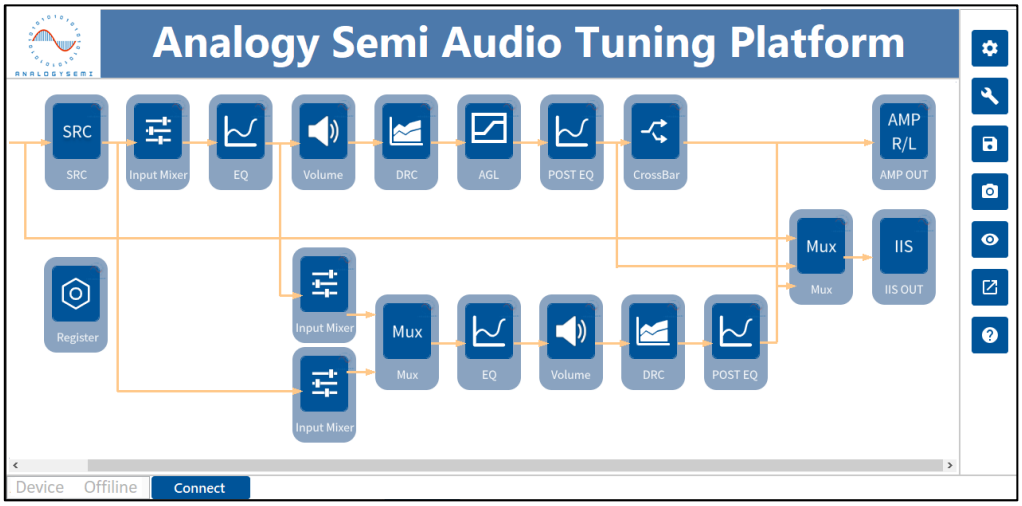


Figure 35. ASATP

11. 电源供电推荐

11.1 DVDD 供电

DVDD 支持 3.3V 和 1.8V，通常建议使用 0.1μF 电容加 4.7μF 电容作为去耦。

11.2 PVDD 供电

PVDD 支持范围为 4.5V-26.4V，一般建议 2 组 PVDD 至少需要 0.1μF 电容加 2 个 22μF MLCC 电容用于去耦。

11.3 布局

请参考 EVM 或者咨询公司销售支持。

12. PACKAGE INFORMATION

The AU6815E is available in the TSSOP28PP package. Figure 36 shows the package view.

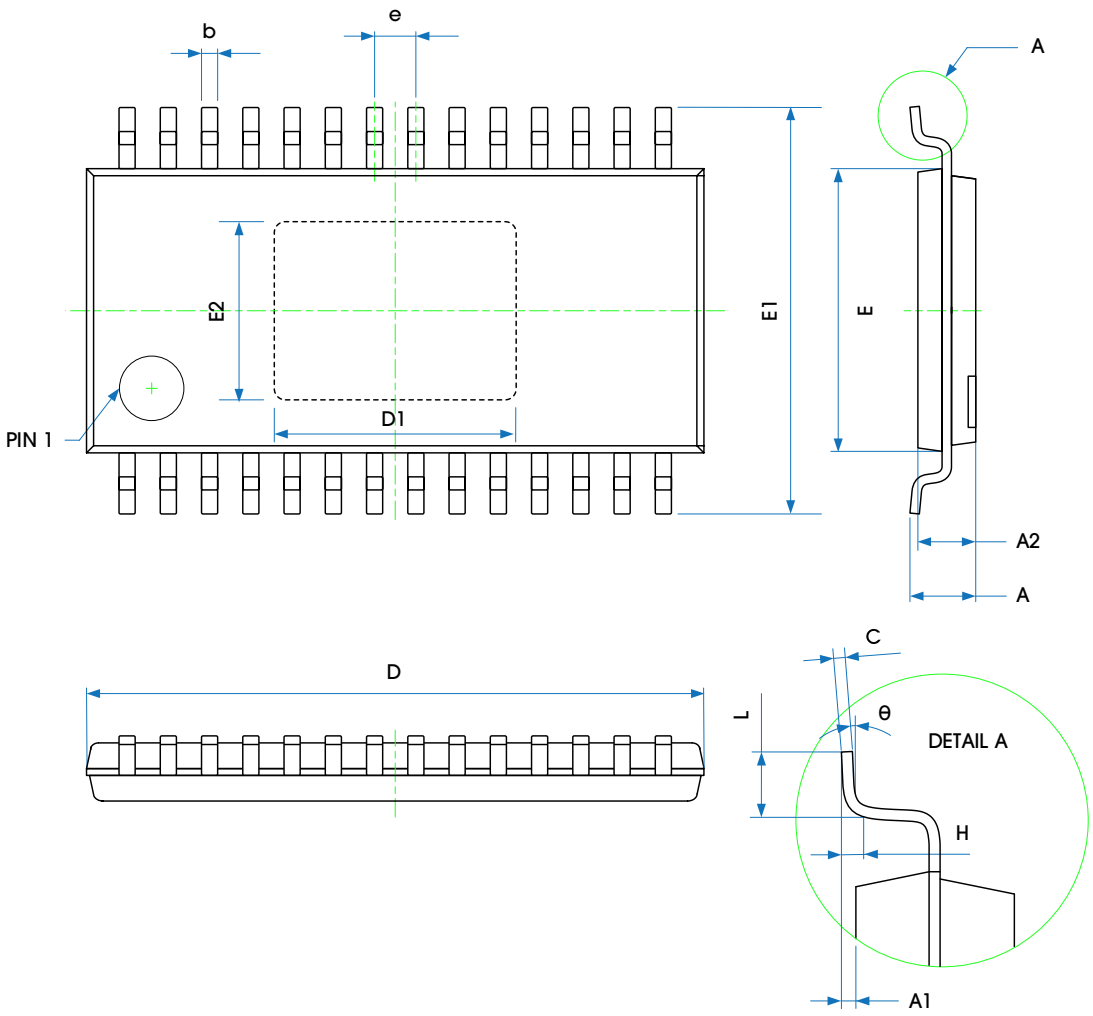


Figure 36. Package View

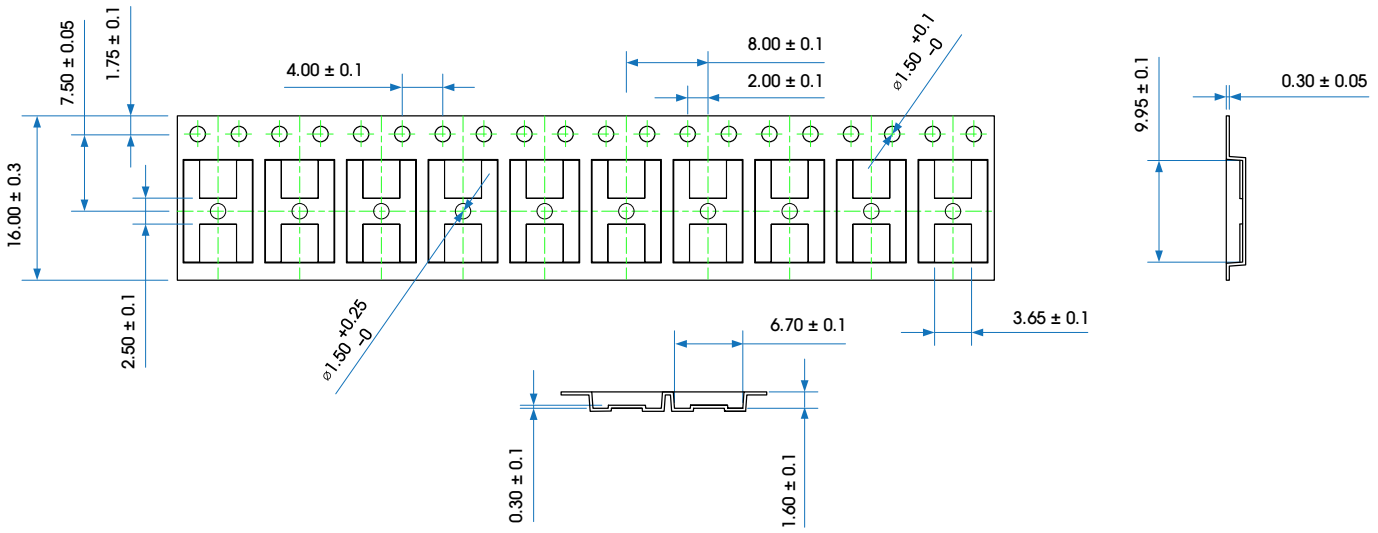
Table 51 provides detailed information about the dimensions.

Table 51. Dimensions

SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
D	9.600	9.800	0.378	0.386
D1	3.710	3.910	0.146	0.154
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
E2	2.700	2.900	0.106	0.122
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.02	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°

13. TAPE AND REEL INFORMATION

Figure 37 illustrates the carrier tape.



Notes:
1. Cover tape width: 16.00 ± 0.3.
2. Cumulative tolerance of 10 sprocket hole pitch: ±0.20 (max).
3. Camber: not to exceed 2mm in 250mm.
4. Mold#: TSSOP28PP.
5. All dimensions: mm.
6. Direction of view:

Figure 37. Carrier Tape Drawing

Table 52 provides information about tape and reel.

Table 52. Tape and Reel Information

PACKAGE TYPE	REEL	QTY/REEL	REEL/ INNER BOX	INNER BOX/ CARTON	QTY/CARTON	INNER BOX SIZE (mm)	CARTON SIZE (mm)
TSSOP28PP	13''	3000	1	8	24000	336*336*48	420*355*365

Figure 38 shows the product loading orientation—pin 1 is assigned at Q1.

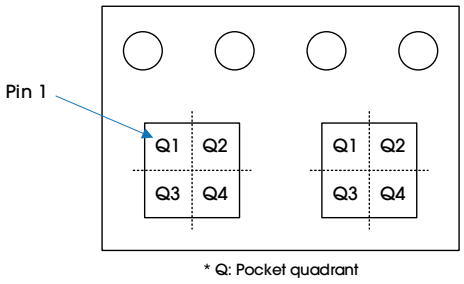


Figure 38. Product Loading Orientation

REVISION HISTORY

REVISION	DATE	DESCRIPTION
Rev A	21 January 2026	Rev A release.